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Supplementary Information

Ion transport and switching speed in redox-gated 3-terminal organic memory devices

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1. Electronic test apparatus

Electronic measurements were made with a Windows desktop computer installed with a National Instruments PCI-6110 simultaneous sampling DAQ board and two Stanford Research Systems SR570 low-noise current preamplifiers to provide a voltage output proportional to the input current for each analog input (AI) channel (Fig. 1). The two analog output (AO) channels of the 6110 board were used to bias the system according to the voltage waveforms generated by the user. Analog output channel AO 0 is connected directly to the source (S) on the sample and controls the source-gate voltage, V_{SG}, since the gate is at virtual ground. Channel AO 1 is connected to the signal ground of the SR570 preamp to control the DC bias at the drain (D) of the sample. This allows D to be biased independently of the S bias, with V_{SD} determined as follows:

$$V_{SD} = V_{SG} - V_D = AO\ 0 - AO\ 1$$

For the “propagation” experiment, both SR570 “low” inputs were grounded, so the D and G both remain at virtual ground potential.

The hardware was controlled using an in-house program built using LabVIEW programming language from National Instruments. The front panel (Fig. 2) allows the user to control the settings on the individual SR570 preamps and determine the specifications of the output voltage waveform based on several waveform generation modules available. The generated voltage waveforms are then passed along the two corresponding analog output channels while the data acquisition occurs simultaneously in the two analog input channels. Once the data acquisition is complete the results are displayed on the front panel and raw results are exported to an Excel spreadsheet.

The SR570 amplifiers have a maximum bandwidth of 1 MHz, with the rise time decreasing from 1 μsec to ~50 μsec as the gain is increased from 1 mA/V to 10 μA/V. The 12-bit A/D converters in the NI 6110 board have a maximum acquisition rate 5 megasamples/sec.

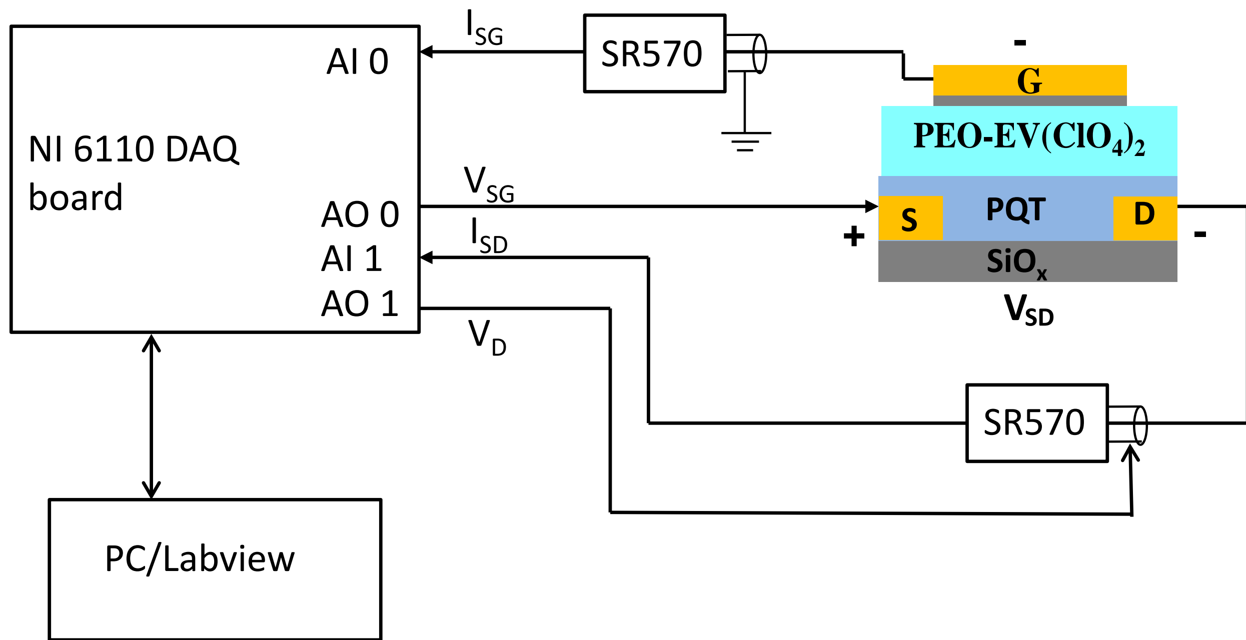

Figure S1. Schematic for dual pulse and propagation experiments controlled by a National Instruments data acquisition board and LabVIEW software. For propagation experiment, V_D was at virtual ground potential.

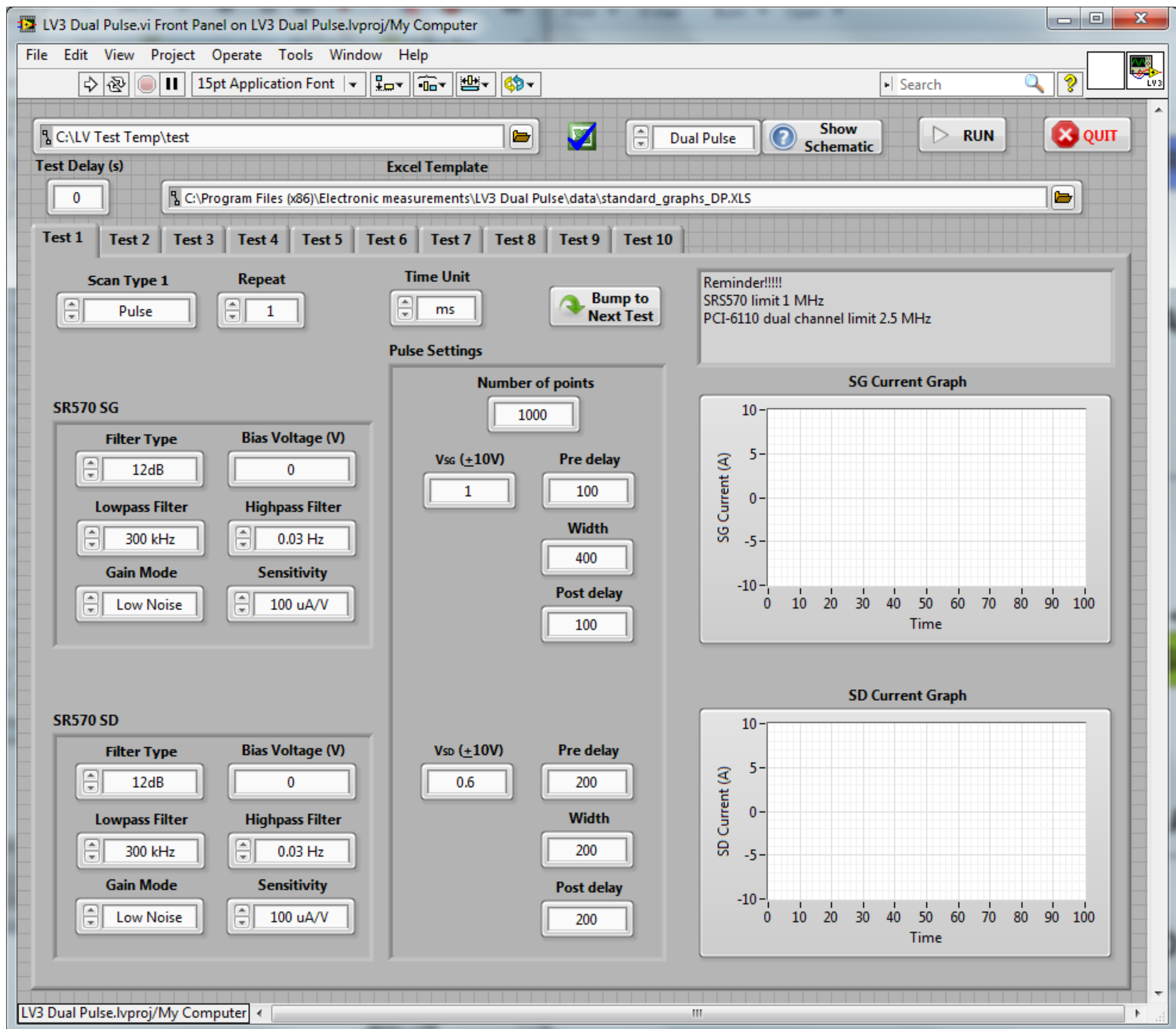

Figure S2. Front panel within LabVIEW for controlling the dual pulse experiment.

2. Time constant determination

Current transients for I_{SG} are shown in Figure 4 of the main text. RC is the inverse slope of the linear plots of ln (I_{SG}) vs time, with the results listed in Table S1. The resistance R for each device was determined from the intercept of ln (I_{SG}) at t=0 and the applied V_{SG} of 0.5 V. “PEO-EVP only” refers to a layer of electrolyte containing $EV(ClO_4)_2$ without PQT present, either spin coated or drop cast as

indicated. “PQT/PEO-EVP” refers to the full stack of drop cast or spin-coated PEO-EVP on a ~30 nm spin coated layer of PQT, as described throughout the main text.

Table S1 Resistance, Capacitance, and RC time constants of various memory devices

Device	Electrolyte layer	Conditions	"RC" (μsec)	R (kΩ)	C (nF)
PEO-EVP only	Drop-cast	Air	2.53	8.75	0.29
		Vacuum	9.39	371.70	0.25
		ACN vapor	4.02	13.59	0.30
PQT/PEO-EVP	Drop-cast	Air	2.44	9.67	0.25
		Vacuum	5.63	375.82	0.15
		ACN vapor	3.73	13.05	0.29
PEO-EVP only	Spin-coat	Air	1.44	1.40	1.03
		Vacuum	1.10	0.44	2.51
		ACN vapor	1.34	0.28	4.77
PQT/PEO-EVP	Spin-coat	Air	1.57	2.07	0.76
		Vacuum	1.10	0.47	2.36
		ACN vapor	1.62	0.59	2.75

3. Retention and cycling behavior

Figure S3a shows 2000 repetitive R/W/R/E cycles for a spin coated device similar to that shown in figure 8b of the main text, but with higher W/E voltage to provide greater stress to the device. Cycle life by this measure was not greatly affected by the higher W/E voltages. Figure 3b shows long term retention after a single W pulse at t=0. The “write” pulse causes I_{SD} to increase from ~50 nA to 10 µA, then both the ON and OFF currents decrease slowly with time. After 14 hours the two states are still distinguishable, although the ON/OFF ratio has decreased significantly.

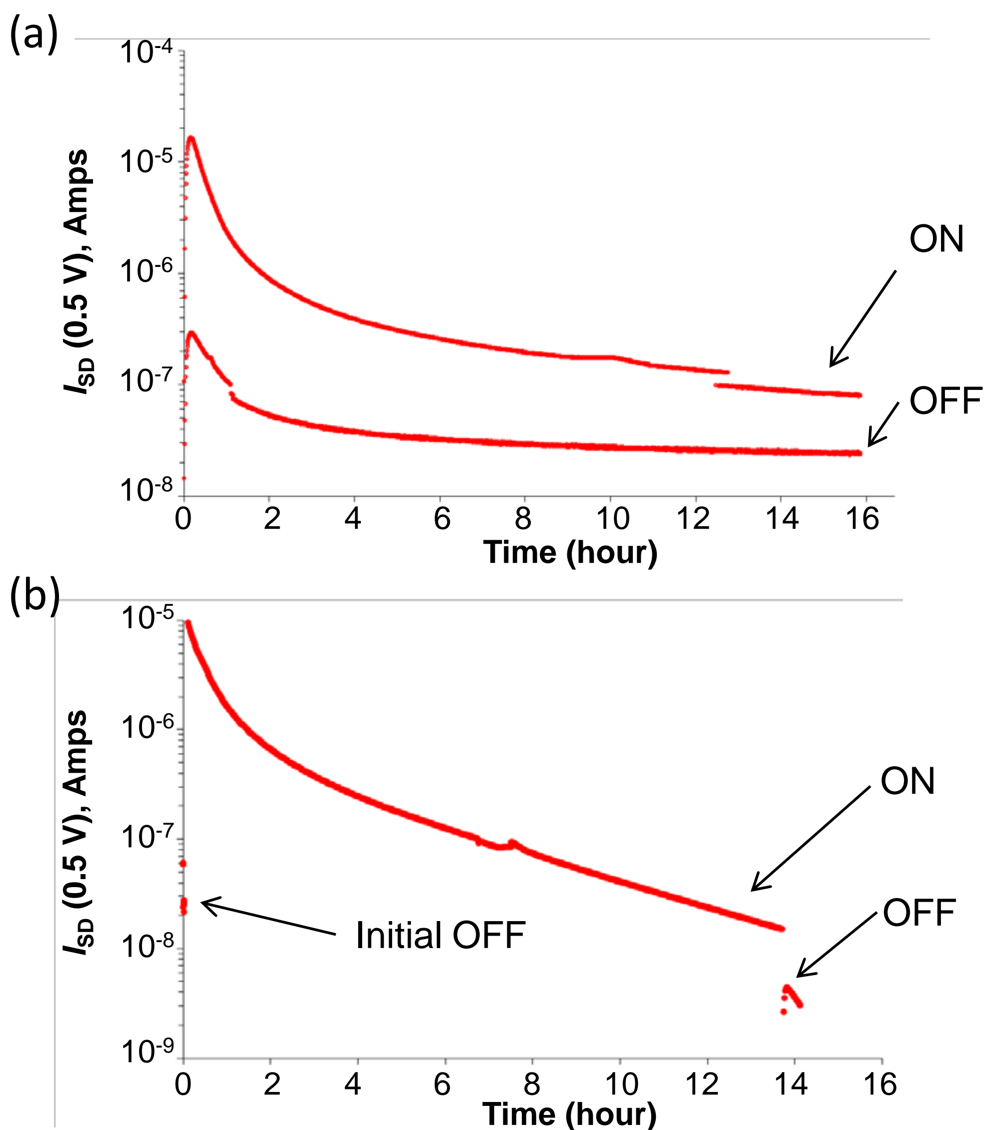

Figure S3: (a) 2000 R/W/R/E cycles of the PQT/PEO-EVP spin-coat device with "write" pulses V_{SG} = + 4 V and "erase" pulses V_{SG} = - 4 V lasting 0.5 sec by repeated for 18 hours in vacuum (~1×10^{-5} Torr). After each write or erase pulse, five consecutive I_{SD} values were recorded at 0.5 sec intervals with V_{SD} = +0.5 V. (b) I_{SD} recorded before and after a single "write" pulse (V_{SG}= +4 V, 2 sec) with I_{SD} sampled at 60 sec intervals by applying V_{SD}= +0.5 V. An "erase" pulse ((V_{SG}= -4 V, 2 sec) was applied after 13.5 hours of repeated readouts.

4. Yield statistics

As noted in the main text, 36 spin-coated Au/PQT/PEO-EV/Au devices on nine different samples were made by two different individuals and compared for ON and OFF currents and memory behavior. Two of the 36 showed visible scratches, and were not examined further. The remaining 34 are shown in figure S4, obtained with V_{SG} pulses of ± 3 V lasting 1 second. Designating devices as "good" when the ON/OFF ratios exceeded 1000, the yield was 29/34, or 85%. The rejected devices showed anomalously high I_{SG} (>10 µA) compared to a typical range of 0.5 -10 µA (e.g. Figure 2a of main text). Defects between the S and G electrode may result in high I_{SG} with minimal oxidation of the PQT.

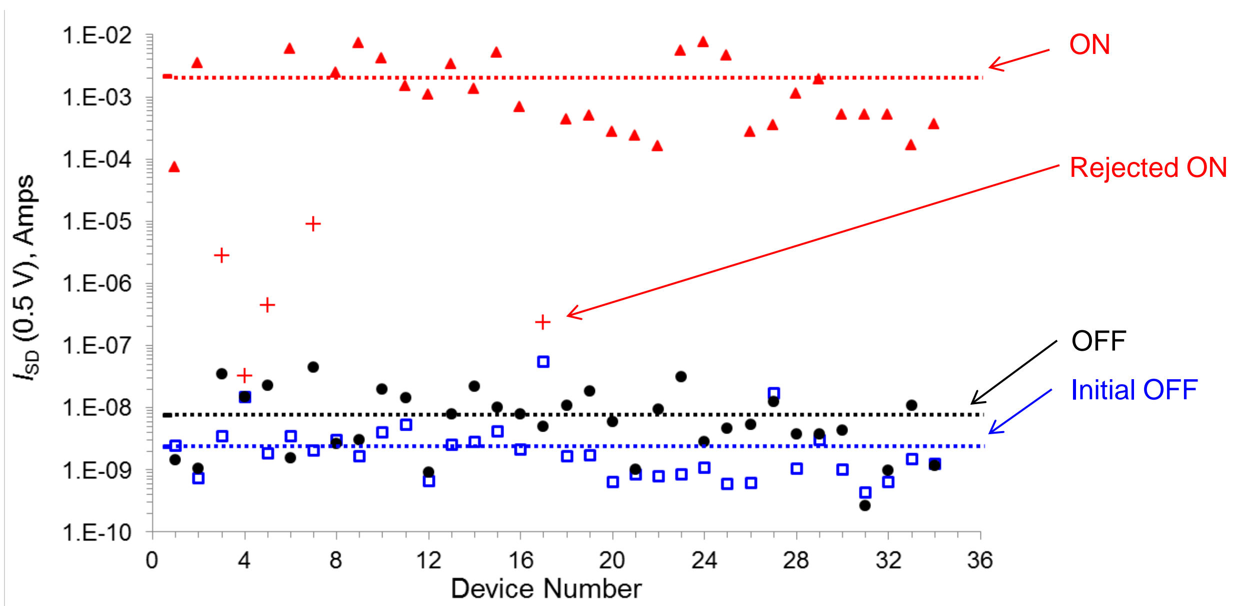

Figure S4: (b) Graphical representation of memory results for 34 devices with 85% yield using On-state, Off-state, & initial Off-state read current. "Rejected ON" indicates devices with an ON/OFF ratio below 1000. Two devices showed visible scratches and are not plotted. V_{SG}= ± 3 V, 1 sec for "write" and "erase" pulses, V_{SD} = 0.5 V.

5. Determination of minimum energy requirements for redox-gated memory devices.

The energy required for a “write” process equals the charge required times the applied V_{SG} bias. If the current devices were scaled down to have a 100 x 100 nm overlap region between the S and G electrodes, approximately 9 x 10^{-19} moles of polaron units (4 polythiophene rings/polaron) would be present in this “cell”. Oxidation of 20% of the four-thiophene ring units to form polarons would require 1.7 x 10^{-14} coulombs, or 1.4 x 10^{-13} C/byte. This yields a predicted “write” energy of 4.2 x 10^{-13} J/byte for V_{SG} = 3 V, or 0.42 pJ/byte. Mathur et al. indicate a range of 17 to 1108 nJ/byte for low power flash memory for erase+write+read operation (Mathur, G.; Desnoyers, P.; Chukiu, P.; Ganesan, D.; Shenoy, P.; Ultra-Low Power Data Storage for Sensor Networks; *ACM Transactions on Sensor Networks* **2009**, *5*, 33). The 100 x 100 nm redox cell would require ~ 1-2 pJ/byte for read+write+erase, and additional overhead might increase the total to 10 pJ/byte. Even with overhead, the redox-gated memory requires less than 0.1 % as much energy as very efficient “flash” memory.