Journal of The Electrochemical Society, **161** (12) H831-H838 (2014)
0013-4651/2014/161(12)/H831/8/$31.00 © The Electrochemical Society

Ion Transport and Switching Speed in Redox-Gated 3-Terminal Organic Memory Devices

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The dynamics of redox gated organic memory devices based on dynamic doping of polythiophene were examined in detail in order to improve "write" and "erase" speed and determine ultimate performance. A 3-terminal geometry similar to a field effect transistor provided a source/gate circuit which reversibly oxidized a polythiophene polymer to cause a large increase in conductance between the source and drain electrodes. The devices were cycled for >1000 complete R/W/R/E cycles, and operated at relatively low voltage compared to commercial "flash" memory. The "write" and "erase" speeds were improved by a factor of >100 by using a spin-coated electrolyte layer and by small increases in device temperature. The influence of charging current and polaron propagation on response time were determined to be minor, with the rate limiting process being identified as the rate of conducting polaron generation. The main factor determining the W/E time was the mobility of ions in the polyethylene oxide electrolyte layer, which resulted in resistance losses during the application of the S-G "write" pulse. Response time was strongly dependent on the atmosphere, with water or acetonitrile vapor significantly increasing the rate of polaron generation. The results are important for design of molecular memory devices based on dynamic doping, and indicate likely avenues for further performance improvements.

Manuscript submitted July 18, 2014; revised manuscript received August 27, 2014. Published September 10, 2014.

The search for alternative nonvolatile memory (NVM) devices continues to be very active, due in large part to the high demand for portable consumer electronics. The dominant solid state NVM today is "flash memory" based on the silicon floating gate field effect transistor geometry, which has high bit density and long retention time (~10 years), but requires high operating voltages and has limited cycle life. Field emission tunneling across a SiOx barrier in "flash" memory requires 10–20 V "write" and "erase" voltages and fatigue of the SiOx layer eventually leads to device failure after several thousand write/erase cycles. Currently used low power "flash" NVM devices require 17–1100 nJ/byte for operation,[1] due in part to a high tunneling barrier necessary for long retention. Many different mechanisms have been investigated for alternative NVM, in both 2-terminal "cross-bar" and 3-terminal configurations, and using organic,[2–4] inorganic,[5–8] and hybrid materials.[9–12] A significant fraction of these alternative NVM devices are based on redox reactions and in some cases accompanying ion motion in solid state devices, which result in changes in device resistance. Various phenomena underlie these resistance changes, including filament formation,[13–16] oxygen vacancy migration,[17–20] and dynamic doping of conducting polymers.[21–28] An advantage of resistive memories is the reliance on conductance changes rather than charge storage, resulting in small cell size and good scaling. In addition, redox events are not dependent on field emission, occur at relatively low operating voltages and require much less energy compared to "flash" memory (as discussed below). Redox reactions have also been proposed to explain performance degradation in organic field effect transistors (OFETs), due to slow and irreversible oxidation of the organic materials assisted by residual moisture or ion motion. Such "bias stress" has been attributed to several phenomena, including trapped charge, proton migration, and reactions with water.[29–33] Although "electrolyte gating" may be used to enhance OFET operation, it is important to distinguish between the "electrostatic doping" used in FET operation and the "electrochemical gating" where persistent redox reactions are responsible for memory operation.[34–37] The former is active only while a gate bias is applied, while the latter persists after a gate bias pulse generates a change in device conductance and is then removed.

Our laboratory has investigated "redox gated" 3-terminal organic memory devices which have a geometry similar to an OFET but a very different operating principle. The 3-terminal structure shown in Figures 1a and 1b separates the write/erase (SG) circuit from the "read" (SD) circuit, thus permitting independent control of redox events and resistance readout. As shown in Figure 1c, a polythiophene polymer (PQT) is spin coated across the Source (S) and Drain (D) electrodes, and its conductivity is monitored by the SD circuit. Above the PQT is a layer of an electron acceptor (ethylviologen diperchlorate, EV), mixed with polyethylene oxide (PEO), then a Gate (G) electrode of carbon and gold. Application of a positive bias above 1.5 V between the S and G electrodes generates polarons (PQT^+) in the PQT layer, accompanied by electrochemical reduction of EV^{+2} to EV^+ and migration of ClO_4^- ions from the PEO to the PQT layers to compensate the positively charged polarons (eq 1 & 2).

$$EV(ClO_4)_2 \rightarrow EV^{+2} + 2 \cdot ClO_4^- \quad [1]$$

$$PQT + EV^{+2} \rightleftharpoons PQT^+ + EV^+ \quad [2]$$

The E^0 values for $PQT^+ \rightarrow PQT$ and $EV^{+2} \rightarrow EV^+$ conversion are +0.76 and −0.45 V vs NHE respectively, so the estimated E^0 for the electrochemical cell using the PQT/EV$(ClO_4)_2$ system is ~1.21 V. An E^0 of 1.21 V represents the bias required to carry out the redox reaction between the S & G electrodes (eq 2). We confirmed this redox gating mechanism by observing PQT polaron formation with Raman spectroscopy,[38] and studied the effects of polymer structure and atmosphere on device performance.[39] The W/E process can be repeated for at least 1000 cycles, and multistate memory is possible by variations in the W/E voltage.[39] Although complete W/R/E/R cycles were repeatable in a vacuum, the W/E speed was significantly faster in the presence of water or acetonitrile (ACN) vapor.[39,40] These redox gated PQT devices should require much less W/E energy compared to "flash" memory, since the redox process has lower power demands than the field emission tunneling required in "flash" memory. For example, the redox reactions in a 100 × 100 nm memory cell based on PQT/EV devices is estimated to require <10 pJ/byte for a "write+read+erase" operation (with $V_{SG} = +3$ V), compared to 17 nJ/byte for an efficient example of "flash" memory in common use currently[1] (see supplementary information). A significant practical problem with the redox gated devices studied previously is relatively slow W/E time compared to commercial "flash" memory. A "write" pulse lasting >10 msec was required in ACN vapor to yield a sufficient change in SD conductance, and this lengthened to >200 msec in air, as reported previously.[39] "Flash" memory in common use has W speeds of ~1–10 μsec and block "erase" times of a few msec, so the W/E speed of the PQT/EV memory devices needs to be significantly faster before commercial applications are considered.

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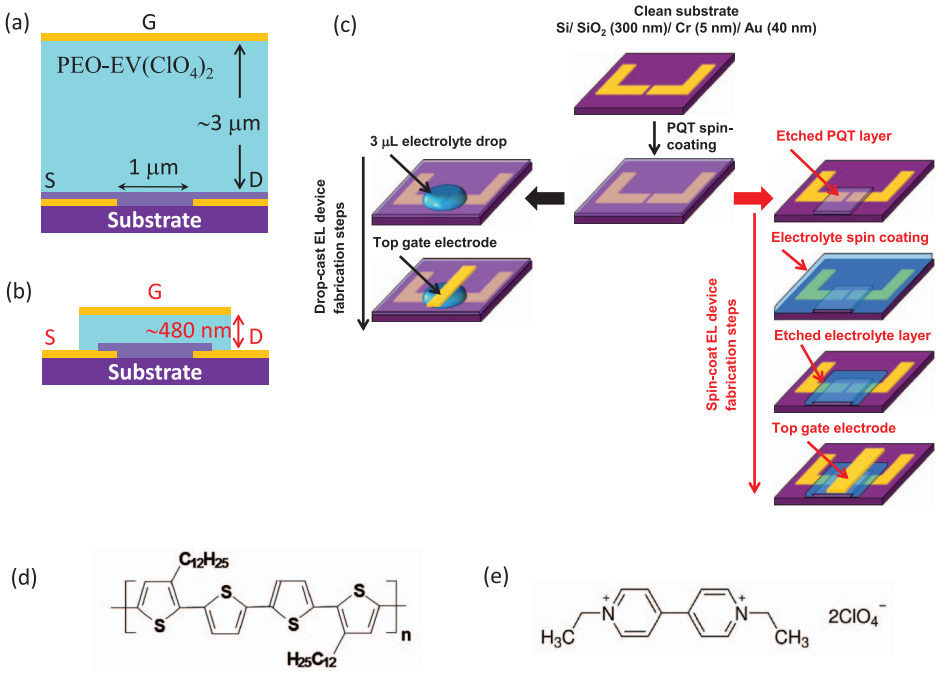

Figure 1. Schematic cross sections of drop-cast (a) and spin-coated (b) memory devices and their fabrication sequences (c). Substrates are Cr/Au on silicon oxide with typically a 1 μm S-D electrode gap. Electrolyte layer is polyethylene oxide containing ethyl viologen perchlorate (e), applied on top of a spin coated active polymer layer of PQT-12 (d).

The current report describes a systematic analysis of the dynamics of redox gated Au/PQT/PEO-EV/e-C/Au memory devices by varying device dimensions, "write" voltage, ambient environment and temperature, in order to determine the factors which constrain the W/E speed. A detailed examination of the solid-state electrochemistry which underlies memory operation was conducted with fast electronics capable of simultaneous monitoring of the W/E operations as well as the change in PQT conductance in the SD circuit. Time resolution down to a few μsec permitted dynamic observation of capacitive charging, polaron formation with associated counter-ion motion, and polaron propagation, thus providing a detailed picture of the entire dynamics of memory operation. In addition, identification of ion motion as one of the rate limiting steps permitted improvement of W/E time to a few msec, as well as an indication of the ultimate speed achievable with the current materials and device dimensions.

Experimental

Chemicals and materials.— Polyethylene oxide (PEO, Aldrich, MW = 100, 000), ethyl viologen diperchlorate (EV, 98%, Aldrich), lithium perchlorate ($LiClO_4$, 99.9%, Aldrich), dimethyl sulfoxide (DMSO, 99%, Aldrich), acetonitrile (ACN, anhydrous, 99.9%, Caledon Laboratories) were used as received. The conducting polymer, regioregular poly(3,3'''-didodecyl-quaterthiophene) (PQT-12), was provided by Xerox Research Centre of Canada as 0.3 wt% dispersion in 1,2 dichlorobenzene. Structures of PQT and EV are shown in Figure 1d and 1e respectively.

Device Fabrication

The details of the fabrication of the memory device made with a drop-cast PEO/EV layer have been reported previously[38,39] and summarized in the left portion of Figure 1c. Briefly, the devices were fabricated on Si/SiO_2 (300 nm) substrates with photolithographically patterned source (S) and drain (D) electrodes which are 0.5 mm wide with a channel gap of 1 μm, except as noted otherwise. The electrodes were prepared by E-beam evaporation of 40 nm Au layer over a 5 nm adhesion layer of Cr. After fabrication, the substrates were inspected using an optical microscope for visible defects or contaminants. The polymers were used as 0.3 wt% solutions in 1,2 dichlorobenzene (PQT and P3HT) and spin-coated on clean Si/SiO_2/Au substrates at 1000 rpm for 120 sec to yield polymer films of comparable thickness (~25–35 nm). Before spin coating the PQT solution was sonicated for 15 minutes at ~80°C. The spin coated polymer films were kept at room temperature overnight in a vacuum at $\sim 10^{-3}$ Torr. The electrolyte solution was prepared by mixing equal weights of 4 wt% ethyl viologen diperchlorate [$EV(ClO_4)_2$] in acetonitrile and 5 wt% PEO in acetonitrile. The PEO solution was filtered through a 0.45 μm PTFE filter before adding the viologen solution. The electrolyte layer was deposited over the dried polymer films by drop casting 3 μL of electrolyte solution in such a way that the electrolyte drop centered on the S-D gap. As shown in Figure 1a, the resulting drop cast PEO films were ~3 μm thick and the spin coated films were 0.48 μm thick including PQT layer thickness (~30 nm). After drying the electrolyte layer in house vacuum ($\sim 10^{-3}$ Torr), the devices were transferred to an electron-beam evaporator (PVD-75, Kurt J. Lesker) for the deposition of gate electrode. The electron beam evaporator was then pumped down to a base pressure of $<3 \times 10^{-6}$ Torr prior to the deposition of the gate electrode. The 1 mm wide gate electrodes, consisting of 15 nm carbon with 30 nm gold as top layer, were deposited by the E-beam evaporation of respective materials through a shadow mask with an evaporation rate of 0.2–0.3 Å/s for carbon (denoted e-C) and 0.5–1.0 Å/s for Au. The e-C layer prevented Au penetration of the PQT/PEO layers, as described previously.[41] As shown in the image of Figure 3a, the gate electrode overlapped the S and D electrodes symmetrically, resulting in overlapping areas of 0.0025 cm^2 each for the S and D electrodes. The samples were stored in a dry nitrogen box prior to their characterization.

A spin coating procedure for the PEO/EV layer was developed, with the process shown schematically in the right portion of Figure 1c. Fabrication of spin coated devices was similar to that for drop casting except for additional steps as follows: Immediately after the PQT layer was spin coated at 1000 rpm for 120 sec, the sample was etched with O_2 plasma through a metal shadow mask to remove PQT in areas outside the S-D region, as shown in Figure 1c. After etching the PQT layer, the samples were kept at room temperature overnight in a vacuum of $\sim 10^{-3}$ Torr. PEO/EV electrolyte (5% : 4% in ACN) was spin coated at 1000 rpm for 60 sec on the PQT patterned substrate. An O_2 plasma etch was used to pattern the electrolyte layer over a slightly larger area than PQT using a different metal shadow mask. Finally, the top gate electrode was deposited using E-beam evaporation through a shadow mask, as was the case for drop-cast devices.

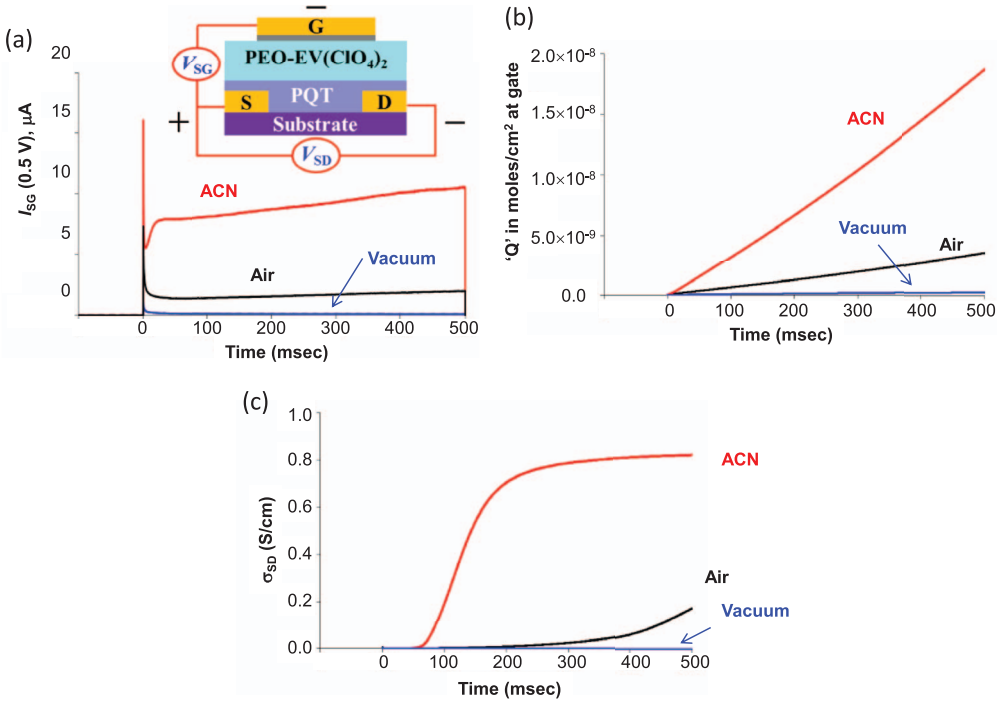

Figure 2. Response of a drop-cast redox gated memory device to simultaneous application of a V_{SG} pulse of +3 V (with S positive) and $V_{SD} = 0.5$ V. (a) Transient current (I_{SG}) between S and G electrodes, with positive sign indicating PQT oxidation, in air, vacuum, and acetonitrile vapor (ACN) as indicated. (b) Total charge passed in SG circuit, in moles/cm^2, equal to the integrated charge divided by the SG overlap area and Faraday's constant. (c) average conductivity (σ_{SD}) of PQT between the S and D electrodes, determined from the transient I_{SD} response recorded during the V_{SG} pulse shown in (a) as $\sigma_{SD} = d_{SD}I_{SD}/(V_{SD}A_{SD})$ where d_{SD} is the gap between S and D electrodes and A_{SD} is the cross-sectional area of PQT between S and D.

Device Characterization

Electronic characterization was carried out with either a Keithley 2602A source measurement unit (SMU) or National Instruments 5 MHz 6110 data acquisition board and Stanford Research SR570 current amplifier using custom software, as described previously,[39] with additional detail shown in Figures S1 and S2 in supplementary information (SI). Device contact was made with probe stations and tungsten probes, in some cases in a Janis Research ST-500–1-VMF-HMF Probe Station. Additional software development with LabVIEW enabled several pulse experiments with μsec time resolution for characterizing memory cell operation and switching dynamics. First, a "dual pulse" experiment simultaneously monitored the S-G (I_{SG}) and S-D (I_{SD}) currents during application of separate voltage pulses to the respective circuits (V_{SG} and V_{SD}). In all cases, positive V_{SG} is defined as a positive 'Source' electrode relative to the 'Gate'. A variation of the dual pulse experiment with a small V_{SG} of 0.5 V permitted observation of the 'RC' charging current decay between S-G without inducing redox reactions, since >1.2 V is required to induce reaction 2 above. A second configuration was used to measure the propagation rate of polarons across the S-D gap during a memory "write" pulse, using the schematic of Figure S1 in SI. A "write" pulse was applied between the S and G electrodes as previously, but two SR570 current amplifiers simultaneously monitored the resulting I_{SG} and I_{SD} currents while keeping the D and G electrodes at virtual ground. The "time of flight" of polarons across the S-D gap was detected as an increase in the I_{SD} current above baseline after the initiation of the "write" pulse. The channel width was varied over a range of values (1, 2,5,10, 20, 40 and 100 μm), keeping all other fabrication and measurement parameters constant.

R/W/E/R memory operation was monitored with a Keithley 2602A SMU as described previously,[39] with the schematic as shown in the inset of Figure 2a. The "read" bias V_{SD} was always 0.5 V, and was applied in between "write" and "erase" pulses. Both I_{SG} and I_{SD} were monitored by the SMU using in-house Visual Basic programs. Repetitive R/W/R/E cycles could be applied for endurance testing, with sub-msec time resolution. All electronic characterization was carried out in one of three atmospheres: air, after $< 1 \times 10^{-5}$ Torr vacuum for >12 hrs, and after 15 minutes in acetonitrile vapor in the Janis probe station following 12 hour vacuum exposure.

Results and Discussion

As noted in the introduction, the Au/PQT/PEO-EV/e-C/Au memory devices with drop-cast electrolyte have attractive power demands, non-destructive resistance readout, good cycle life, and high ON/OFF ratio, but unacceptably slow W/E times. Since electrochemical redox reactions often occur on a submicrosecond time scale in solution and on modified electrodes,[42,43] the source of the slow response in the solid state is not obvious. We conducted several experiments with the drop-cast devices in order to determine the origin of the slow W/E response, and improved speed significantly with thinner, spin-coated electrolyte layers. The I_{SG} responses of a drop-cast device in the three atmospheres are shown in Figure 2a, and consist of an RC charging spike followed by the polaron generation current. Figures 2b and 2c show the total charge passed in the SG circuit and the resulting SD conductivity which accompany the I_{SG} pulses. The conductivity was determined for the PQT layer between the S and D electrodes, which starts at a low, "undoped" value of $\sim 10^{-4}$ S/cm. Although all three cases show "write" times of >100 msec, there is a strong dependency on atmosphere. At least three phenomena may limit the rate of the SD current change: (i) RC charging time, (ii) polaron generation rate with counter ion motion, and (iii) polaron propagation from the S to the D electrode. These will be considered in turn below, with attention to how atmosphere affects "write" speed. Since ion transport is likely involved in controlling redox reaction dynamics, we also examined spin coated electrolyte layers, in which the PEO/EV thickness was reduced from ~3 μm to 0.48 μm, presumably with similar reduction in electrolyte resistance.[44] Spin-coating of electrolyte on the PQT-12 layer proved difficult due to the hydrophobic nature of the PQT surface. With the procedure shown in Figure 1c, the combination of PQT layer patterning by plasma etching, electrolyte spin coating and again

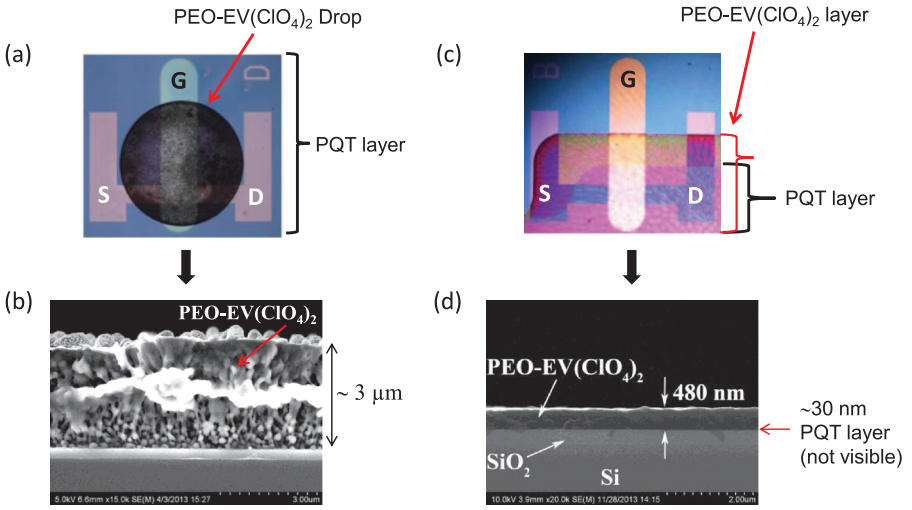

Figure 3. (a) Optical image of top of finished spin coated memory device, with the G electrode on top of the dried, drop-cast PEO-EV film. (b) SEM cross section after cleaving through the region between the S and G electrodes. (c) Completed spin-coated device, defined in part by the etching steps shown in Figure 1c, and its SEM cross section (d). PQT layer is ~30 nm thick in all cases, and not visible.

plasma etching to pattern the electrolyte enabled successful fabrication of the spin coated devices shown in Figure 3c. The area of the patterned PEO-EV layer is slightly larger than that of PQT layer to avoid direct contact between PQT-12 and gate electrode, and possible conductance through PQT between the G and S or D electrodes. As shown in the SEM cross sections of Figure 3b and 3d, the spin coated PEO layer is thinner and more uniform than the drop-cast films, with reasonably planar interfaces and a total thickness of 480 nm.

Figures 4a and 4b show the transient response of I_{SG} in response to a 0.5 V V_{SG} pulse, in order to evaluate the time required for charging the RC circuit between the source and gate, for air and ACN vapor respectively. The small V_{SG} pulse amplitude avoided significant redox activity, so that an exponential current decay is expected. Figures 4c and 4d show linear regions for plots of ln(I_{SG}) vs time which indicate RC time constants of 1–4 μsec for both spin cast and drop cast devices. Although the time constant varies with atmosphere and device type, the RC time constants were < 4 μsec for drop-cast and spin coated devices in air or ACN vapor. Detailed analysis of the RC behavior of all cases studied is provided in table S1 in SI, and the observed time constants are all much faster than the >50 msec "write" times apparent in Figure 2c. The < 5 μsec time constants for the relatively large cells studied here not only indicate that RC charging is much faster than the observed slow "write" times but also that RC charging should not be a speed limitation in the much smaller cells in any practical memory application.

A second factor controlling speed is the rate of polaron generation at the positively biased S electrode during a "write" pulse, which depends on the rate of electrochemical oxidation of PQT, following possible Ohmic potential losses in the electrolyte layer. A direct indication of this rate is provided by the currents recording during "write" operation, shown in Figure 2a. The initial spike near t = 0 corresponds to RC charging, and does not depend strongly on

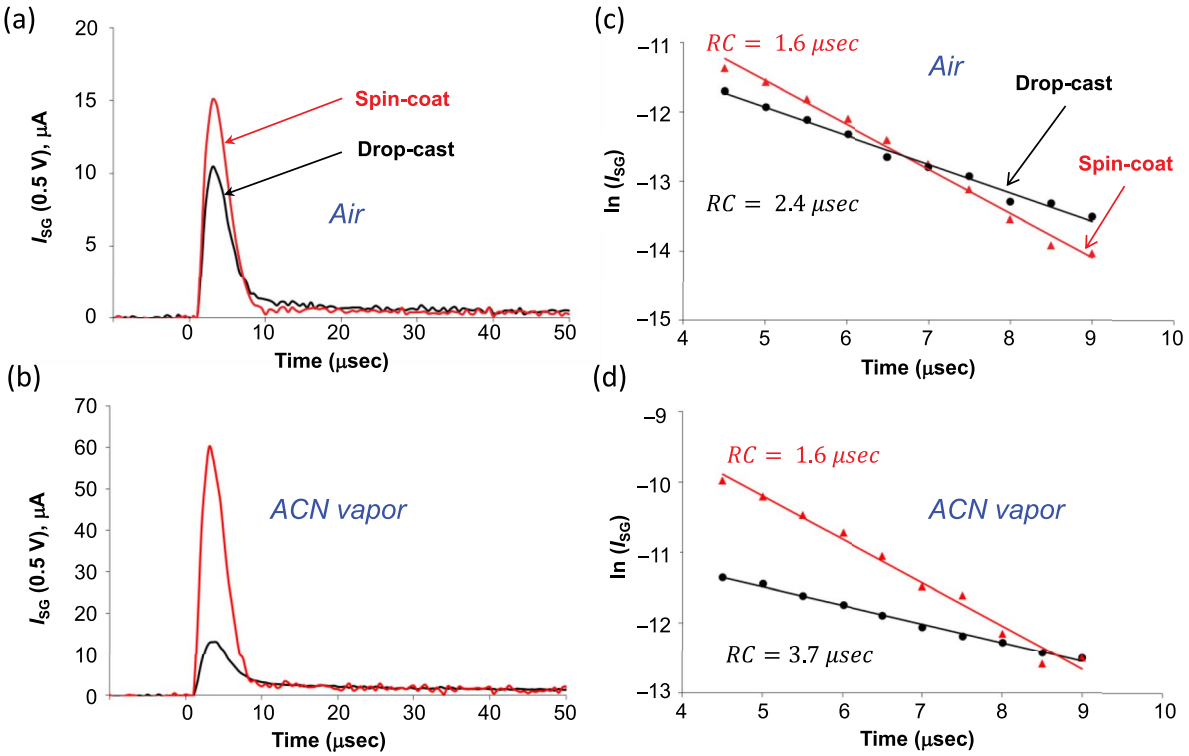

Figure 4. Fast I_{SG} response resulting from V_{SG} pulse of 0.5 V in air (a) and ACN vapor (b) for drop cast (black curves) and spin coated devices (red curves). (c) and (d) show the linear regions of ln (I_{SG}) vs time, with the corresponding RC time constants determined from the inverse slope of the lines.

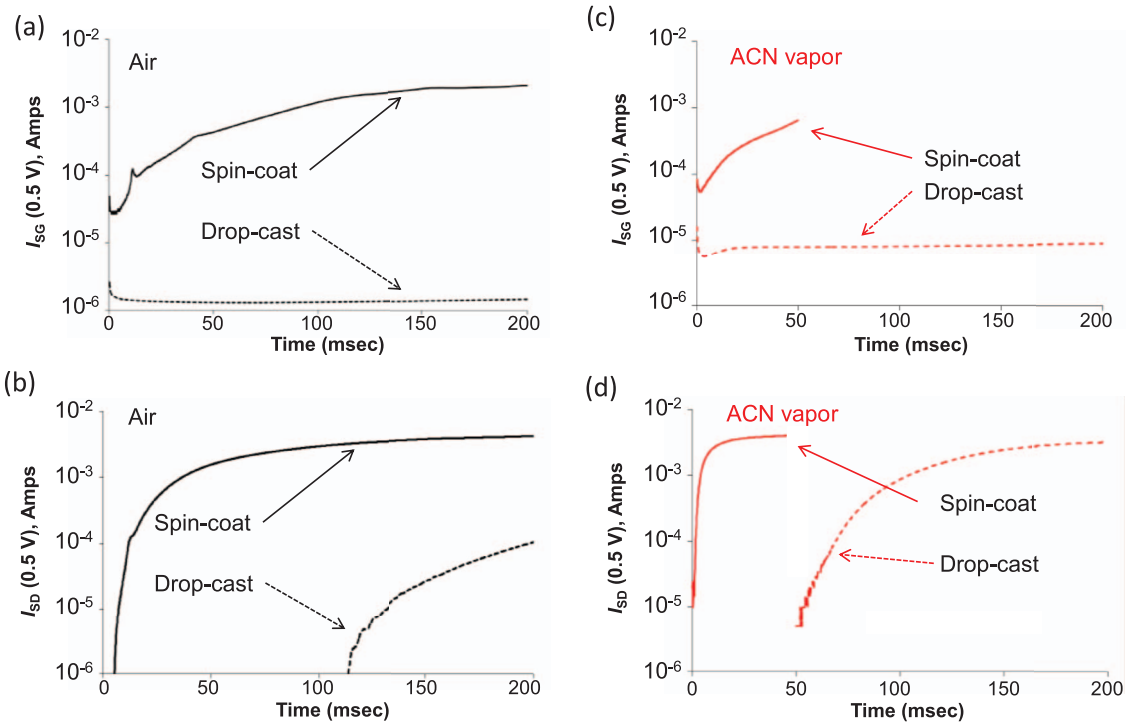

Figure 5. (a) Transient I_{SG} response for drop-cast and spin-coated devices during simultaneous "write" (SG)" and "read (SD)" dual-pulse measurements in air, with $V_{SG} = +3$ V and $V_{SD} = 0.5$ V. (b) Corresponding transient I_{SD} responses for same experiment as (a). (c) & (d) Same experiments as (a) & (b) on same devices, but after >12 hours in vacuum and ~15 minutes in acetonitrile vapor.

atmosphere, as noted above. I_{SG} following the RC spike is generating polarons Faradaically, and shows a strong dependency on atmosphere, with polarons generated approximately 50 times faster in ACN vapor compared to a vacuum, as indicated by the much higher I_{SG} current in ACN vapor. Figure 2b shows the charge passed during the "write" pulse, in moles/cm^2 of the overlapping area of the S and G electrodes. The 30 nm thick PQT film contains approximately 9×10^{-9} moles/cm^2 of polaron units, assuming four thiophene rings/polaron. Therefore, a 200 msec "write" pulse is oxidizing at most ~20% of the PQT (~2×10^{-9} moles/cm^2) over the S electrode in air, but ~100% in ACN vapor. The continuing increase in oxidation charge up to 500 msec and beyond in Figure 2b is due to propagation of polaron into the gap region and around the perimeter of the S electrode, and will be discussed below. Based on Figures 2a and 2b, it is clear that polaron generation rate is at least partially responsible for slow "write" operations. From the conductivity change between the S and D electrodes plotted in Figure 2c, approximately 200 msec and > 5×10^{-9} moles/cm^2 of charge are required to reach maximum PQT conductivity in ACN vapor, with much slower response in either air or vacuum.

A major improvement in "write" speed resulted from decreasing the thickness of PEO/EV layer from 3 μm in the drop-cast devices to 0.48 μm in the spin coated samples, as shown in Figure 5. Note first that the I_{SG} current is >100 times larger in the spin coated samples (Figure 5a), corresponding to a >100x increase in the rate of polaron generation. A plot of I_{SD} on a log scale shows the much faster "read" response of the spin coated devices (Figure 5b). Similar benefits of spin coating are retained in the ACN atmosphere (Figure 5c and 5d), with further decrease in response time after a "write" pulse. The variation of current responses with V_{SG} has diagnostic value for determining the origin of the major improvement in "write" speed with spin coating, with the results shown in Figure 6. Dual pulse experiments were conducted for a V_{SG} range of 3–5 V for 100 msec, much longer than the RC decay time and including much of the time required for I_{SD} to increase from its initial low value. As shown in Figures 6a and 6b, I_{SD} for the drop-cast devices show a strong dependency on V_{SG}, while the spin-coated samples do not. As apparent in Figure 6c, I_{SG} at t = 100 msec for drop-cast device shows a linear dependency on V_{SG} for the range of 3–5 V, indicating a differential resistance in this region of 2.5 MΩ in air and 0.25 MΩ in ACN vapor. For spin-coated samples in air, I_{SG} and I_{SD} decrease slightly with increasing V_{SG}, indicating that electrolyte resistance and PQT oxidation rate are no longer limiting the device response. These results imply that uncompensated resistance losses are important in the relatively thick drop-cast PEO-EV layer, but not in the spin-coated devices. The decrease in electrolyte thickness in the spin-coated devices has decreased the large Ohmic potential losses present in the drop cast devices to values which no longer affect the polaron generation rate in the spin-coated devices.

Once the polarons are generated at the S electrode, they propagate into the S-D channel, by a combination of redox exchange and a "moving" electrode represented by the conducting front of PQT polarons. As noted previously, this propagation is accompanied injection of ClO_4^- from the PEO/EV layer to compensate the charge of the PQT polarons. As shown schematically in Figure 7a, the propagation rate was determined by monitoring both I_{SG} and I_{SD} while a +3 V pulse was applied to the S electrode, in a series of seven devices with varying SD gaps of 1 to 100 μm. Figure 7b shows the current responses for the cases of 1 and 10 μm channel gaps. The +3 V pulse was initiated at t = 0, and produced an I_{SG} response similar to the usual "write" process, for both 1 and 10 μm gaps. The D electrode at ground potential in this case is acting as a detector of polarons after they traverse the SD gap, with the rise of I_{SD} from its resting value (~0) indicating the arrival of polarons at the D electrode. The delay time, taken as the time required for I_{SD} to reach 1.0 μA, is ~5 times longer for the 10 μm gap compared to the 1 μm gap. The I_{SD} transients for various gaps are shown on a log scale in Figure 7c, and the delay times required for I_{SD} to reach 10 nA and 1 μA are plotted in Figure 7d. The observed average speed is 6–8 μm/msec, indicating that polarons can propagate through a 1 μm S-D gap is less than 1 msec. Although the minimum propagation time may be an impediment to the ultimate speed of redox-gated memory, it does not explain the >100 msec lag in I_{SD} response for the drop cast devices in air.

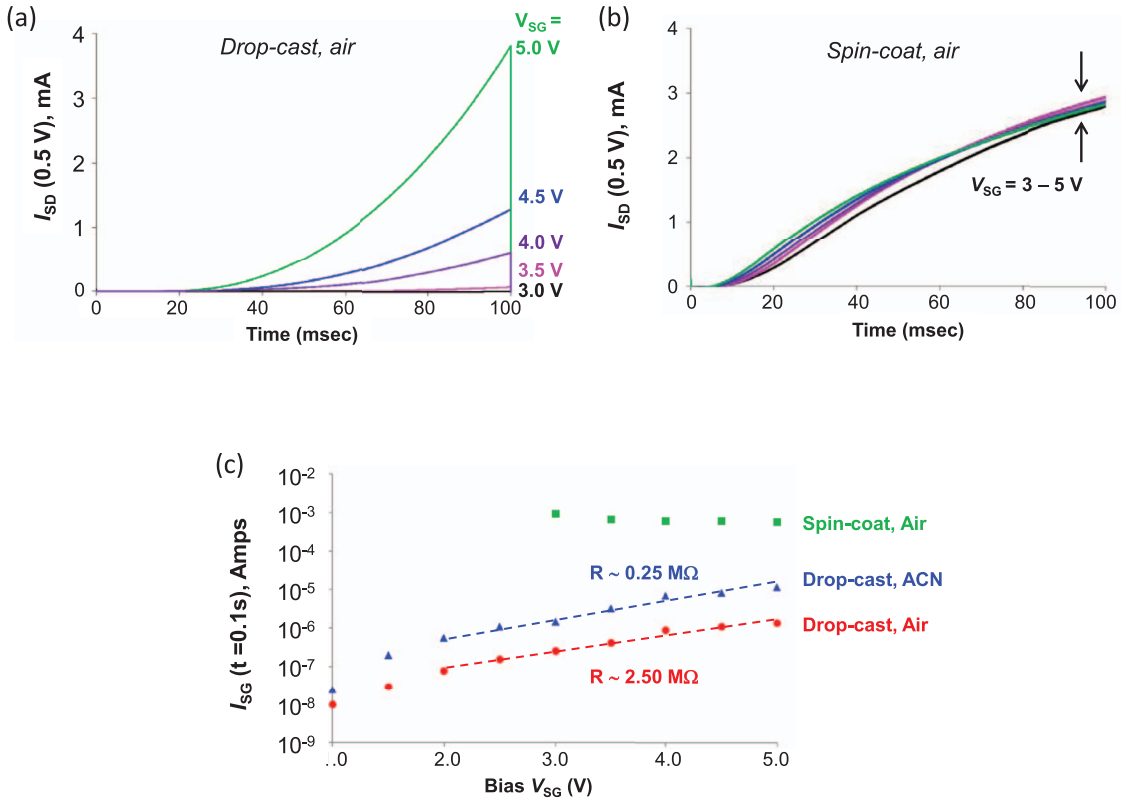

Figure 6. Effect of V_{SG} on the I_{SD} response for the indicated conditions for drop-cast (a) and spin-coated (b) devices in air. (c) I_{SG} (at t = 100 msec) vs V_{SG} for the cases indicated. R values were determined from the slopes of the lines shown. I_{SG} showed a small decrease with increasing V_{SG} for spin-coated devices, implying negligible resistance.

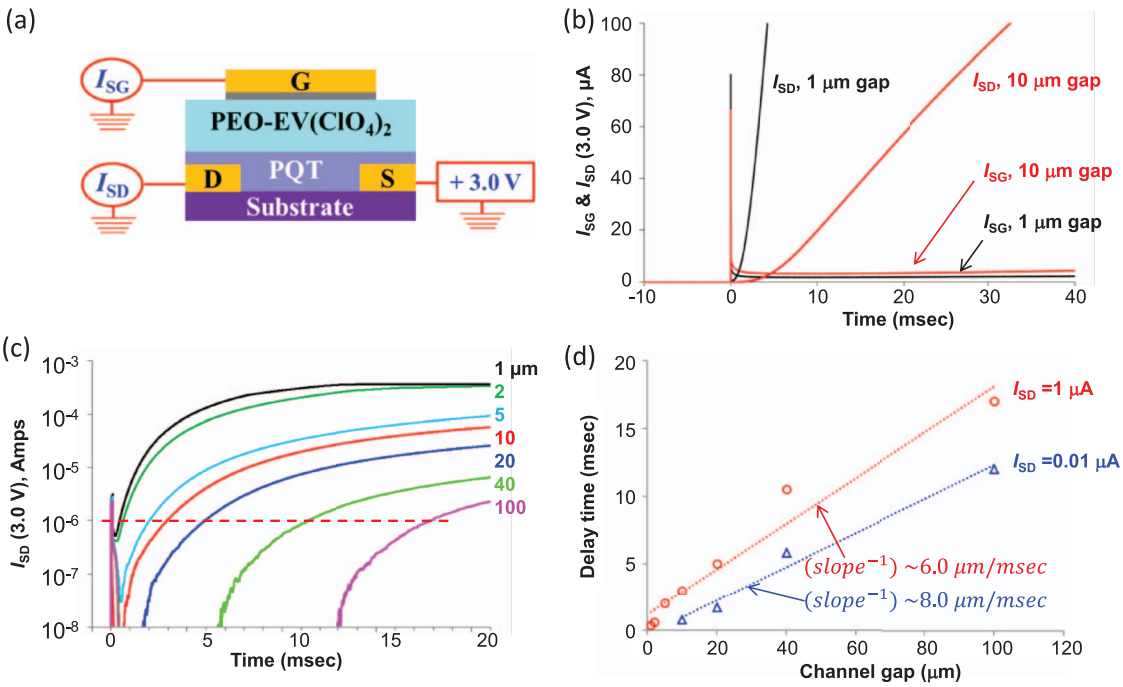

Figure 7. (a) Schematic of propagation experiment, with I_{SG} and I_{SD} monitored simultaneously while +3 V is applied to S electrode. (b) I_{SD} and I_{SG} vs. t responses for 1 and 10 μm channel gaps. (c) I_{SD} vs. t on log scale for channel gaps from 1 to 100 μm as indicated. (d) Delay time after onset of V_{SG} for I_{SD} to reach a fixed value (1 μA or 0.01 μA) for all seven devices, with the inverse slope indicating an average propagation rate of 6–8 μm/msec. Dashed line in (c) indicates an I_{SD} of 1.0 μA, and the corresponding delay times for varying gap width.

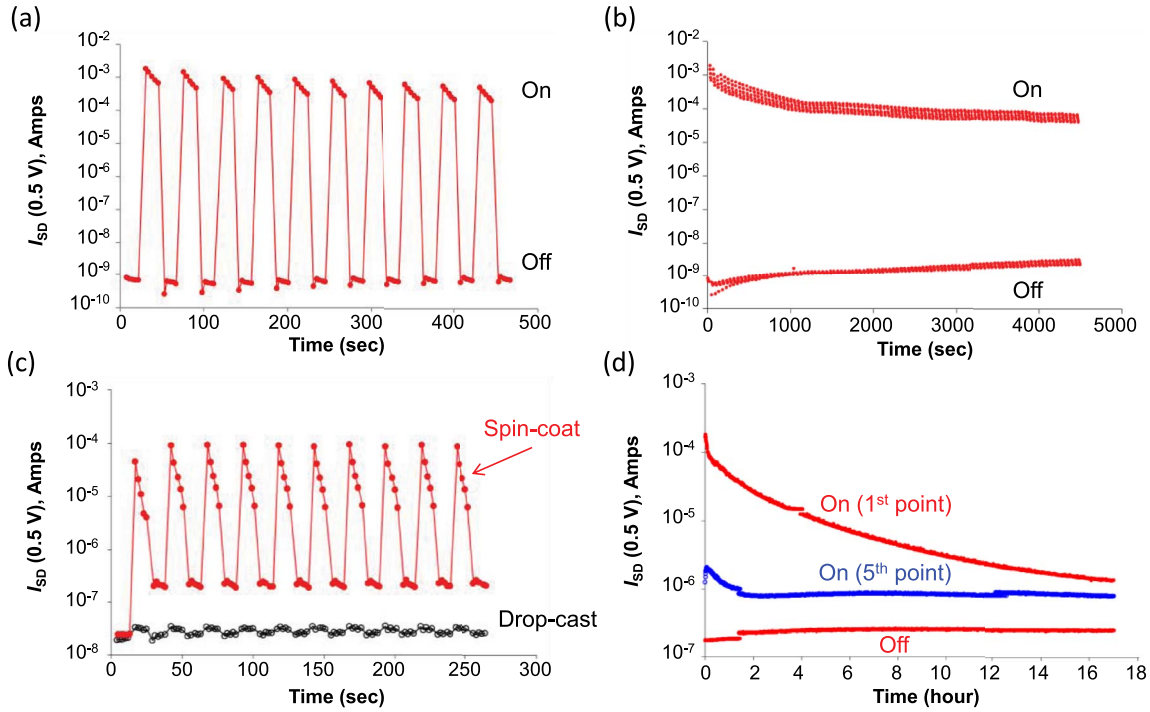

Figure 8. (a) Initial 10 R/W/R/E cycles for a spin coated memory device in air. "write" pulse was +3 V, 1 sec, "erase" pulse was –3 V, 1 sec, and readout pulse was +0.5 V for 2 seconds. (b) Repetition of the same sequence for 100 complete cycles. (c) Memory cycles with 10 msec W and E times for drop-cast and spin coated devices in ACN vapor at room temperature with other parameters the same as in (a). (d) 2000 R/W/R/E cycles with the parameters of part (c) except ±4.0 V W/E pulses, shown for the 1st and 5th point after completion of the "write" pulse, and first point after "erase".

Figure 8 shows repetitive R/W/R/E cycles for spin coated devices using slow pulse parameters (1 sec, +3 V "write") for 10 (Figure 8a) and 100 (Figure 8b) memory cycles, with results similar to those for the drop cast devices. Figure 8c compares the two configurations (both drop-cast & spin-coat) for 10 msec "write" speeds, showing that ON/OFF ratios exceeding 100 are possible with W/E pulses too short for the drop cast case. Figure 8d shows 2000 memory cycles on a spin coated device with 10 msec W/E pulses, showing both the initial "read" after the "write" pulse and the 5th readout occurring 10 seconds after the end of the W pulse. Although the ON/OFF ratio decreases with repeated cycling, the ON and OFF states are clearly differentiated after 2000 cycles covering >16 hours. The decrease in ON/OFF ratio apparent in Figure 8c with time after the W pulse is due to the redox recombination reaction at the PQT/PEO interface, as noted previously.[39] Figure S3a shows memory cycles for spin coated devices with greater "stress" with $V_{SG} = +4$ and –4 V and 0.5 sec W/E pulses, indicating that the device remains viable after 2000 cycles in vacuum. Figure S3b shows the device behavior following a single $V_{SG} = +4$ V, 2 second "write" pulse to test retention. The ON/OFF ratio decreases with time, but the two states are distinguishable after 14 hours. Future experiments involving a separator layer between the PQT and PEO-EV layers should significantly increase retention. Device yield and reproducibility were assessed by comparing 36 spin-coated devices on nine different samples made by two different individuals, with the results shown in figure S4. Defining a working device as one with an ON/OFF current ratio >1000, the yield was 85%. The rejected devices showed low ON current and anomalously high I_{SG}, possibly due to defects between the S and G electrodes. The effect of a small increase in temperature on memory performance is shown in Figure 9a for spin coated devices in an ACN atmosphere. Note that the I_{SD} exceeds 3 mA at 2 msec after the initiation of the +3 V "write" pulse at 57°C, which significantly exceeds the current observed after 100 msec at room temperature (Figure 5d). The activation energy associated with the temperature dependency may be estimated by an Arrhenius plot of log(I_{SD}) vs 1/T shown in Figure 9b for 1, 2, and 3 msec after the "write" pulse initiation. Although a detailed study of activation energies was not conducted, the observed activation energies of 1.0 to 1.7 eV are similar to those determined from published results for ions in PEO, i.e. 0.7 eV for $NH_4SO_3CF_3$[45] and 1.1 eV for $LiClO_4$.[46]

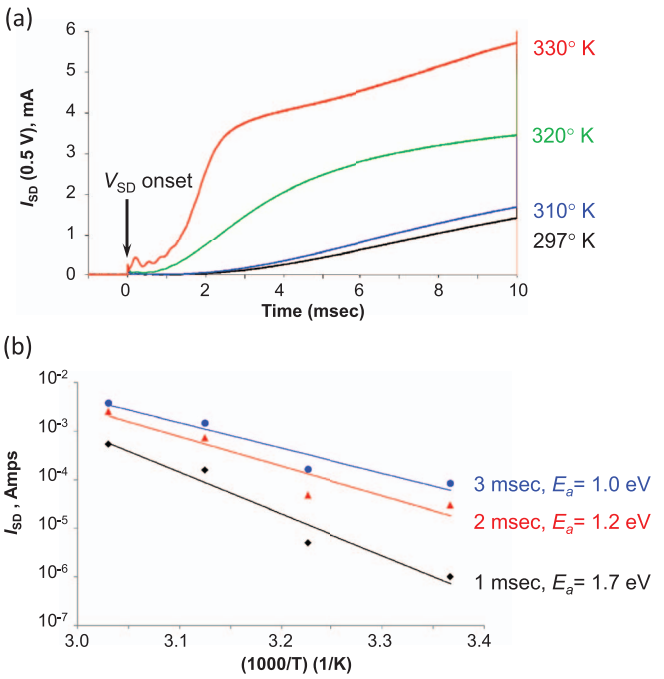

Figure 9. (a) Transient I_{SD} responses for +3 V, 10 msec "write" pulses for spin coated devices exposed to ACN vapor for the temperature range of 297–330° K. (b) Arrhenius plots of I_{SD} at t = 1, 2, and 3 msec, with the corresponding activation energies, E_a.

Finally, some observations about device scaling and speed are useful, based on the geometry of the cell and the properties of the materials involved. RC charging is not likely to be a limiting factor for "write" and "erase" times down to well below a microsecond. RC does not change with device area, but decreases with thinner electrolyte layer and higher ionic conductivity. Many examples of electrochemical redox processes which occur in the submicrosecond time scale have been reported,[42,43] and the "write" voltage may be increased to overcome possible Ohmic or electron transfer rate limitations. Based on the ∼7 μm/msec propagation rate observed for the 1 μm SD gap (Figure 7d), the propagation time should decrease to ∼4 μsec for a 25 nm SD gap, and may be faster for higher conductivity electrolytes. The energy requirements decrease for smaller cells, with the estimated <10 pJ/byte predicted for a 100 × 100 nm cell being much less than the >10 nJ/byte required for conventional "flash" memory (see supplementary information). Based on these estimates, it is likely that redox-gated memory devices can operate with submillisecond W/E times and require much less energy than existing "flash" memory. Operation in the few μsec range is at least feasible without major changes in design or materials.

Conclusions

To summarize the results regarding switching dynamics of redox gated memory devices, the main speed limitation in drop cast devices is the slow generation of conducting polarons due to ohmic losses in the PEO/EV electrolyte layer. The RC charging time and propagation of polaron across the 1μm SD gap are much faster than polaron generation in this case, and not significant factors in device W/E speed. Although increased V_{SG} can partially overcome the ohmic loss in the electrolyte, it was much more effective to reduce the PEO resistance by exposure to ACN vapor and/or decreasing the PEO thickness by spin coating. For the case of spin coated PEO/EV, ohmic losses are no longer rate limiting for V_{SG} above 3 V, and the "write" speed decreases from >100 msec for drop cast devices to less than 10 msec for spin coated samples. The "write" speed is further reduced to ∼ 2 msec in ACN vapor at an elevated temperature of 57°C. The observation that the fastest "write" speed observed to date (Figure 9a) is similar to the minimum propagation time across the SD gap (Figure 7d) implies that the rate limiting step is now polaron propagation rather than polaron generation. An obvious approach to further improving the W/E speed of the redox-gated devices is reduction of the SD gap, which is feasible by at least an order of magnitude with commonly used photolithographic techniques.

The low operating voltage and energy demand compared to existing "flash" memory are attractive features of the redox gated memory devices described here, and the organic and polymeric materials employed may enable applications in "printable" or flexible organic electronic devices. The increase in speed in an acetonitrile atmosphere is likely an effect on ion mobility rather than electrode kinetics, since the speed improvement in spin coated samples has little dependency on applied voltage. Further increases in speed should be possible with higher mobility polymer electrolytes using different mobile ions and/or added plasticizer.[46] A significant remaining issue with the current devices is the relatively short retention, which is caused by redox recombination at the interface between PQT and PEO/EV layers. This problem is normally addressed by including a separator layer which is an ionic but not electronic conductor, and the several year shelf life of many practical solid state batteries is an indication that a separator can greatly increase retention. The detailed analysis of device dynamics presented here should be valuable for designing and refining the electrolyte, separator and electron acceptor components of a redox-gated molecular memory cell.

Acknowledgments

This work was supported by the National Institute for Nanotechnology, the Natural Sciences and Engineering Research Council of Canada, Alberta Nanoworks, and the Xerox Research Centre of Canada (XRCC). The authors thank Nikola Pekas and Xiangyu Chen for assistance with developing the spin coating procedure for the electrolyte layer.

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