Supporting Information for

Redox Gated Three-terminal Organic Memory Devices: Effect of Composition and Environment on Performance

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1. Schematics for Keithley 2602 Source Measurement Unit and LabVIEW interfaces

Figure S1 shows the schematic for the interface between 3-terminal memory devices and the Keithley 2602A dual source measurement unit. The shield of the input to the current amplifier on the D electrode was biased to permit independent control of the SG and SD bias values. The 2602A was controlled by "Test Script Builder" code in the 2602 and visual basic within Excel in the PC computer controlling the experiment.

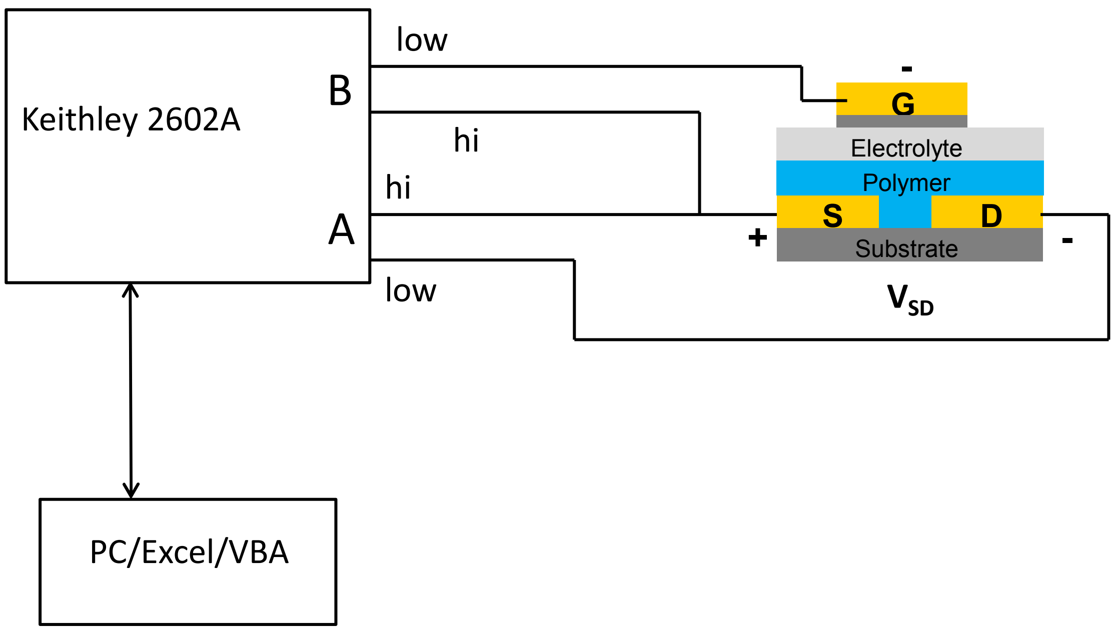

Figure S1: Schematic for Keithley 2602A Source Measurement Unit interface to redox gated memory device. "A" and "B" indicate channels of 2602, with polarities indicated. The circuit permitted independent control and measurement of the S-G and S-D bias and currents.

Figure S2 shows the schematic for the LabVIEW interface, consisting of a National Instruments 6110 DAQ board with two analog outputs (AO) and two analog inputs (AI). A custom program in LabVIEW was used to control the experiment and acquire data.

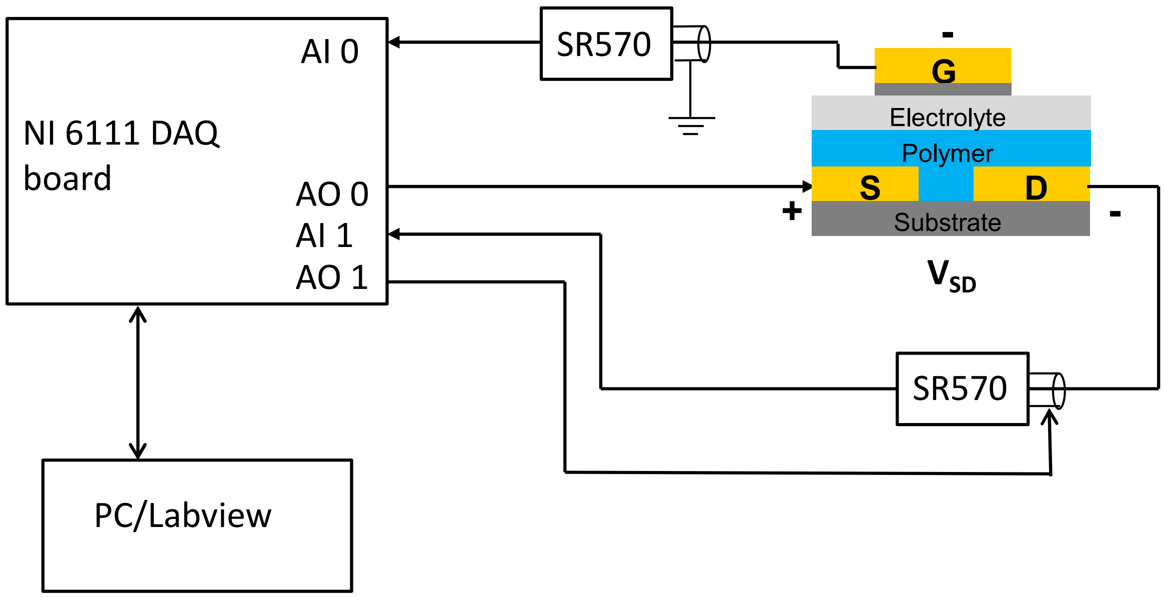

Figure S2: Schematic for the National Instruments LabVIEW interface to redox gated memory device. SR570 is a Stanford research current amplifier, NI6110 is a 5 MHz data acquisition board in a personal computer, AO indicates analog outputs from the DAQ board, and AI indicates analog inputs. The circuit permitted independent control and measurement of the S-G and S-D bias and currents with significantly faster time resolution than the Keithley 2602. Note that AO1 provides a bias to the D electrode.

2. Two-terminal *I-V* responses for P3HT and Polystyrene devices

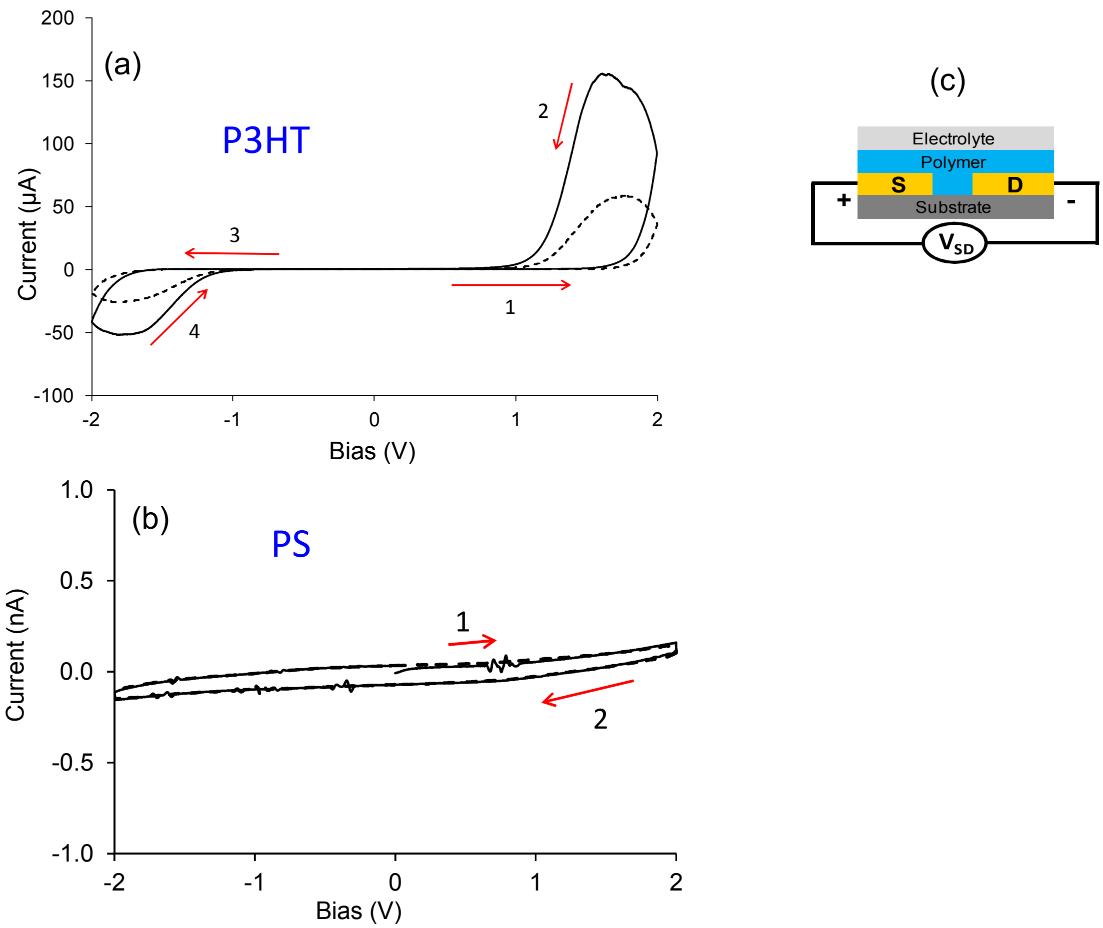

Figure S3: Two terminal (SD) *I-V* sweeps for P3HT (a) and PS (b) open-face devices obtained with sweep rate of 20 mV/s. The bold lines are the first cycle and the dotted lines are the second cycles. The structure of the test devices is shown in panel (c). Note the large difference in current scale between (a) and (b).

3. Two-terminal *I-V* responses for PQT with varying electrolyte layer

Figure S4 shows 2-terminal *I-V* scans for PQT devices with different or absent electrolyte layers. The current for PQT alone is very low, since the polymer is initially in the reduced state (S4c). Scans of a PQT/PEO device lacking EV also exhibit very low currents (S4b), but including EV in the PEO results in an increase in current of more than three orders of magnitude.

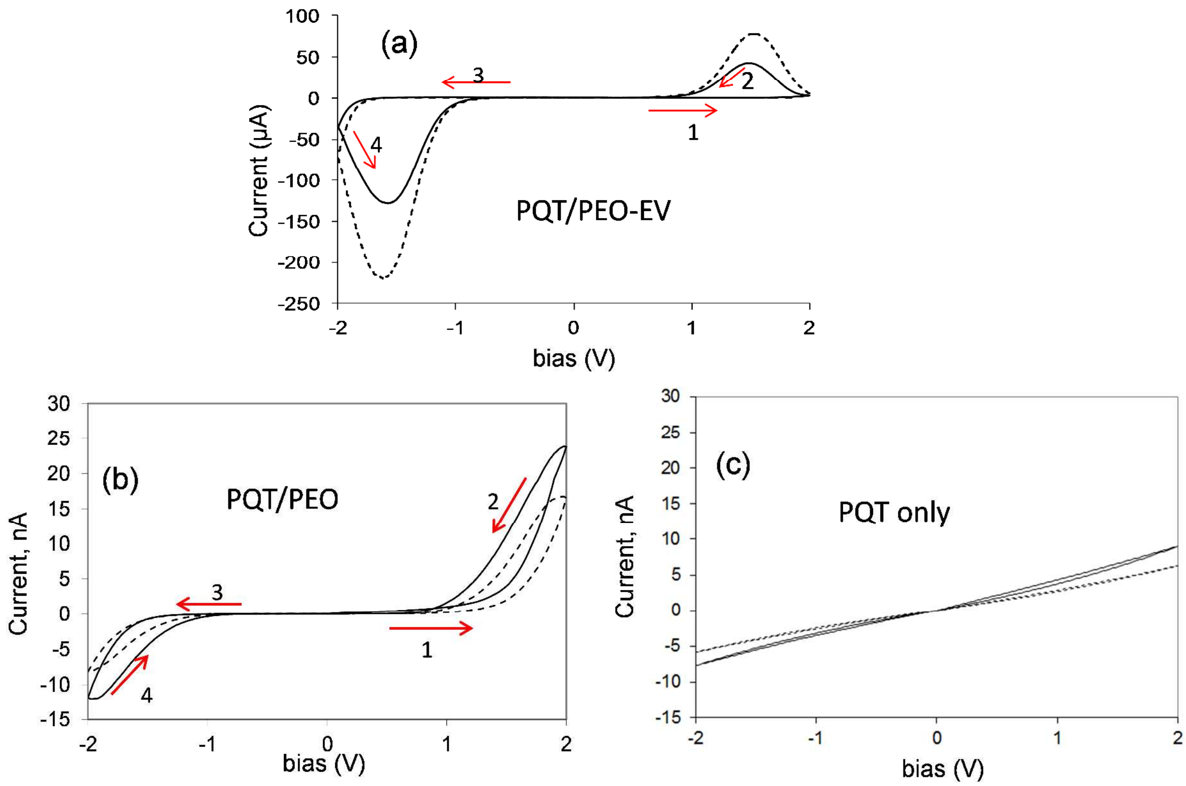

Figure S4: Two terminal (SD) *I-V* sweeps for PQT-PEO only open-face device obtained with sweep rate of 20 mV/s. The solid black line is the first loop and the dotted black line is the second loop. The structure of the test devices are as shown in Figure S3(c). Note the large difference in current range for (a), compared to (b) and (c)

4. 1000 R/W/R/E memory cycles of three-terminal memory devices in air and vacuum

Figure S5 shows 1000 repetitive R/W/R/E cycles for 3-terminal PQT/PEO-EV devices in air (red curves) and vacuum (black curves). The "readout" current for a SD bias of 0.5 V is shown after each "write" pulse (+4 V) to yield the ON state and "erase" pulse (-4 V) to yield the PFF state.

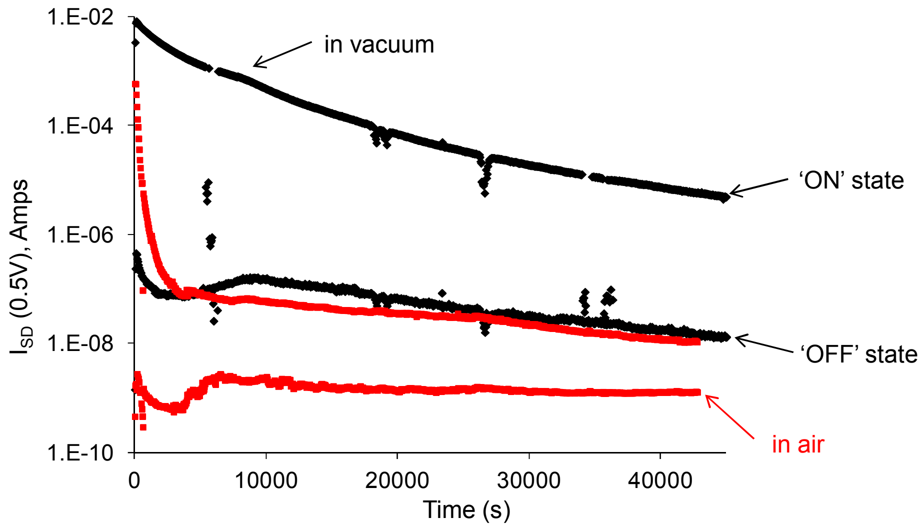

Figure S5: Comparison of endurance of PQT/PEO-EV devices in air and vacuum showing approximately 1000 W/R/E/R memory cycles. The data represent the variation of SD 'readout' currents after a 4V SG 'write' or 'erase' pulses of 2s duration. Both devices were fresh at the beginning of each experiment, conducted in vacuum (black lines) and air (red lines)

5. 2000 R/W/R/E memory cycles of three-terminal memory devices with partial recovery

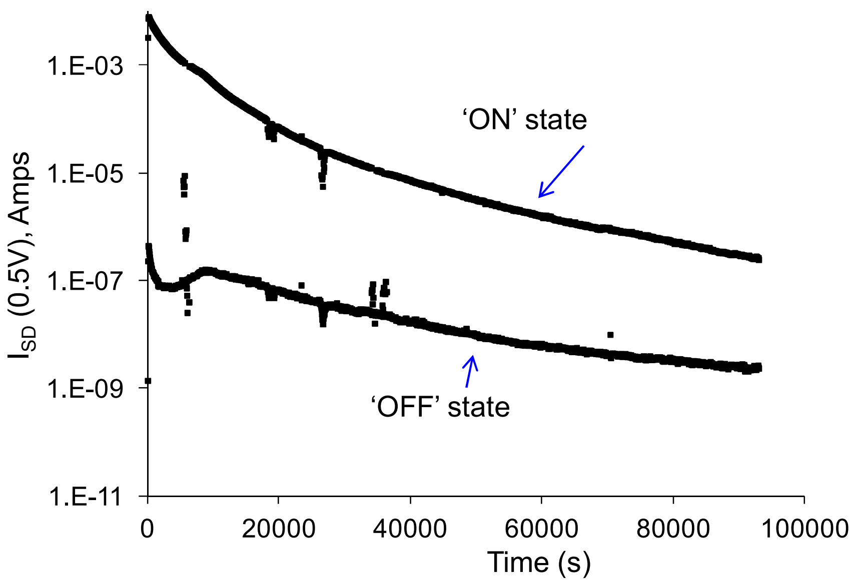

Figure S6: Endurance test of PQT/PEO-EV device in vacuum showing 2000 W/R/E/R memory cycles. The data represent the I_{SD} 'readout' current recorded after each +4V SG 'write' or -4V 'erase' pulses of 2s duration.