Microelectronic Engineering 88 (2011) 3256–3260

Contents lists available at SciVerse ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Thermal oxidation as a simple method to increase resolution in nanoimprint lithography

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ARTICLE INFO

Article history:
Received 10 March 2011
Received in revised form 12 July 2011
Accepted 11 August 2011
Available online 30 August 2011

Keywords:
Thermal oxidation
Resolution
Master fabrication
Electron beam lithography
Nanoimprint lithography

ABSTRACT

We introduce a simple thermal oxidation technique for decreasing feature sizes of nanoimprint lithography (NIL) masters. During oxidation, the dimensions of negative features are reduced (e.g., gaps become narrower), and the dimensions of positive features increase (e.g., lines become wider). We demonstrate that positive feature sizes can also be reduced after oxidation by selective etching of the oxide. We show that 74 nm gaps can be reduced to 10 nm and 226 nm lines can be narrowed to 55 nm. The reduction in feature size achieved in both positive and negative structures directly translates into increased imprint resolution, and we demonstrate improved resolution in a complete NIL pattern transfer using thermally oxidized NIL masters.

1. Introduction

Nanoimprint lithography (NIL) is a conceptually simple method for patterning high resolution features on a substrate [1]. For pattern transfer with the NIL technique, a rigid master with patterned surface relief features is pressed into a soft "resist", which assumes the negative of the master's pattern. To optimize the process, the imprint pressure and temperature can be varied, and the sample can be exposed to UV or other wavelengths during the procedure. With NIL, high throughput patterning can be achieved, and features with resolutions as low as 5 nm have been successfully demonstrated [2–5]. Due to these attributes, the International Technology Roadmap for Semiconductors (ITRS), the key reference document of the semiconductor industry, has begun to include NIL among the possible methods for reaching the sub-22 nm technology nodes beyond the range of conventional photolithographic techniques [6]. Should the specifications for speed, overlay accuracy, defect density and resolution be met, NIL could become the preferred technique for fabricating the next generation of integrated circuits. In addition, applications with less stringent process requirements also exist, as demonstrated by reports detailing the application of NIL to solar cells [7–10], lighting [11,12], displays [13] and molecular electronics [14]. As a result, NIL is expected to become an increasingly prominent tool in both academic research and in full-scale manufacturing.

As the NIL process involves one-to-one pattern transfer, the imprint resolution is limited by the master, and improvements made to the master can be expected to lead to improvements in the imprinted substrates. Commonly, NIL master fabrication is performed through high resolution electron beam lithography (EBL), followed by reactive ion etching (RIE) [1]. For EBL, fabrication of dense or large area patterns becomes difficult at sub-30 nm resolution due to surface charging, electron scattering in the resist, and aberrations in the electron optics [15–17]. In addition, high aspect ratio RIE to form the master relief pattern becomes increasingly difficult with smaller features, leading to limiting phenomena such as aspect ratio dependent etching (ARDE) [18]. Techniques to increase the resolution of NIL masters most often involve pushing EBL to its limits by, for example, introducing specialized resists or employing Gaussian beam pattern generation, data biasing, and thin resists/masks [19–21]. Other techniques to realize extremely high resolution NIL masters can also involve unconventional non-EBL fabrication routes [2–4].

In this paper, we discuss a simple thermal oxidation technique which circumvents the scaling issues associated with the EBL/RIE fabrication route and allows improved resolution of fabricated NIL masters. Scattered reports of oxidation techniques to vary feature dimensions have previously appeared in the literature, but only in regard to different applications: for example, gate leakage

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doi:10.1016/j.mee.2011.08.006

is reduced in thin film transistors with oxidized channels [22–24], the light emission spectra of Si nanoparticles shift when resized by thermal oxidation [25], the photoluminescence of porous silicon varies with oxidation [26], and the dimensions of microfluidic channels or nanocolumns can also be controlled through thermal oxidation [27,28]. This article demonstrates oxidative resizing as applied to NIL masters. We present a series of Si masters where the minimum feature size is successively reduced through thermal oxidation, and we demonstrate that these masters can be successfully employed for pattern transfer in an otherwise standard NIL process. With this technique, reduction of feature sizes is shown for both negative (e.g., gaps) and positive (e.g., lines) features, and we discuss oxidation conditions and geometrical issues that must be understood in order to generate selected patterns. Several advantages of thermal oxidation are also presented including the reduction of line edge roughness [29–31], and the provision of an OH-rich surface for easy attachment of common release agents [32]. Since the growth of SiO_2 is highly controllable through thermal oxidation [33–35], reduction in feature sizes is achieved with a high degree of precision, and oxidation is demonstrated to be an inexpensive technique to significantly ease the design constraints for the fabrication of high resolution, high density NIL masters.

2. Experimental

The process flow chart for fabrication of an NIL master is shown in Fig. 1. A highly doped, 100 mm, p-type Si wafer (0.005 Ω cm) was cleaned in piranha solution (1:1 H_2O_2:H_2SO_4, note: this is an extremely dangerous solution which should be handled with caution), and the native oxide was removed in buffered oxide etchant (BOE). Poly(methylmethacrylate) (950 kg mol^{-1}, 2 wt.% in anisole, MicroChem Corp.) was spin coated onto the wafer at 4000 rpm and soft baked at 170 °C for 5 min, resulting in a 90 nm thick resist layer. EBL was used to pattern the resist with features in the 70–500 nm range. The resist was exposed at 100 μC cm^{-2} at 10 keV, then developed in 1:3 methyl isobutyl ketone:isopropanol. Etch masks were formed through the evaporation of 2 nm Cr and 15 nm SiO_2 on the EBL-patterned substrate followed by lift-off in dichloromethane. The etch mask pattern was transferred into the Si substrate by RIE in an inductively-coupled plasma reactive ion etcher (ICP-RIE). The ICP-RIE was used in a continuous flow or "unswitched" method with a constant flow of C_4F_8 (60 sccm) and SF_6 (80 sccm) and an RF power of 750 W. The final etch depth was 300 nm with a slightly positive etch profile of 88°. Following the Si etch, the Cr/SiO_2 etch mask was removed with BOE and chrome etch (Anachemia Science, #0906015). The etch profile and feature sizes of the NIL masters were determined by scanning electron microscopy (SEM, Hitachi S-4800) in conjunction with image analysis using the ImageJ 1.40 g software package. Reported feature sizes are averages from ⩾15 positions on a particular lithographic feature, together with the standard deviations from these measurements.

Thermal oxidation of the Si NIL masters was accomplished with a Jipelec Jetfirst Rapid Thermal Annealer (RTA) in a dry O_2 environment at 1000 °C, where fast ramp rates allowed precise control of the oxidation time. Oxide thickness was determined *ex situ* by SEM and ellipsometry (Micro Photonics, EL X-01R), and the change in feature sizes was measured by SEM. For the reduction of positive features (i.e., to reduce line width), the Si NIL master was thermally oxidized in the RTA and then etched in BOE to remove the SiO_2 layer.

A Nanonex 2500 imprinter was used for thermal NIL. A 100 mm Si wafer was cleaned in piranha solution and spin coated with 100 nm of NXR1025 thermal resist. To reduce the adhesion between the NIL master and resist after thermal set, the master was modified by immersion in a 2% (w/w) solution of trichloro-(1H,1H,2H,2H-perfluoroctyl)silane (Aldrich, 97%) in toluene for 30 min. Imprinting was performed at 130 °C and 200 psi for 2 min, followed by demolding at room temperature. After imprint, the resist pattern was extended into the Si wafer using an ICP-RIE etch process identical to that stated above.

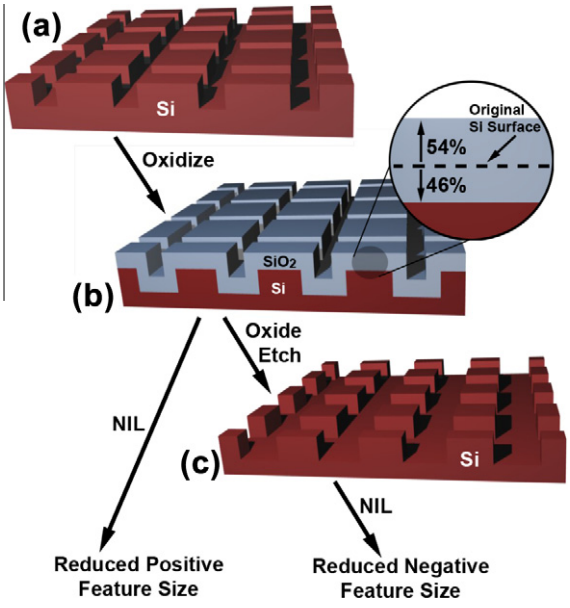

Fig. 1. Process flow diagram depicting the oxidation technique for improving NIL resolution. (a) A moderate resolution Si master is produced by EBL and ICP-RIE techniques. (b) Thermal oxidation of the Si master reduces the size of negative features, with 54% of the oxide formed outside the original Si surface. (c) BOE etching of the oxidized master reduces the size of positive features, since 46% of the thermal oxide forms beneath the original Si surface, and this is removed during etching. These oxidation-processed masters are used in NIL to imprint features (positive or negative) beyond the resolution of the original Si master.

3. Discussion

For dry thermal oxidation of Si, oxygen diffuses through the forming SiO_2 to the Si/SiO_2 interface where it reacts. Since the volume of SiO_2 is greater than that of Si, the growing SiO_2 layer extends beyond the original Si surface. Using the original Si surface as a reference, 54% of the thermally-grown oxide extends outward (i.e., beyond the original dimensions of the Si), while 46% extends inward [36], as shown in Fig. 1. The 54% of the SiO_2 thickness that extends outward from the original surfaces reduces the size of negative features such as gaps and increases the size of positive features such as lines. The final dimensions of these features are controlled by growing the SiO_2 to a predetermined thickness; a process made straightforward by advanced Si oxidation models [33–35,37]. In these models, the oxidation rate is initially large, but drops rapidly and stabilizes at a near-constant rate. For all our experiments, 1000 °C was chosen as the oxidation temperature, and the final oxide thickness fell within the linear portion of the oxidation curve. Although not employed here, *in situ* ellipsometry could also be used to gain additional control over the final oxide thickness.

In Fig. 2, we demonstrate that thermal oxidation can be employed to reduce the width of an initial 74 ± 5 nm gap (Fig. 2a) to less than 10 ± 2 nm (Fig. 2b). Observable in Fig. 2b, the thermal oxide appears darker than the native Si. With the nano-gap geometry, the gap reduction from 74 to 10 nm required 32 nm growth from each sidewall. Since 54% of oxide extends beyond the original Si dimensions, 32 nm feature expansion correlates with a total SiO_2

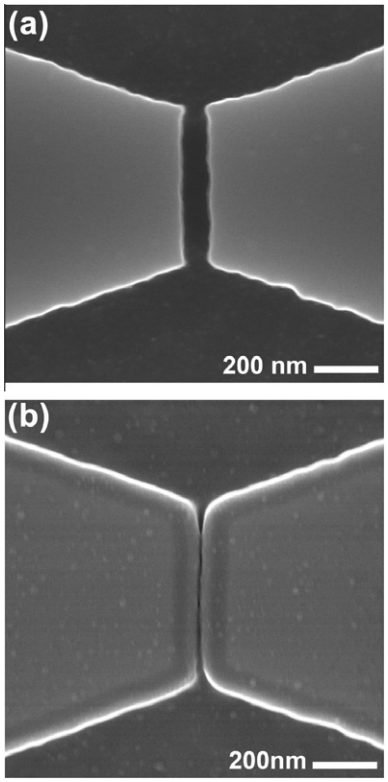

Fig. 2. SEM images of master features resized through oxidation. (a) A 74 nm gap in a Si master formed by EBL. (b) After growing a 55 nm thermal oxide on the Si, the 74 nm gap is reduced to 10 nm.

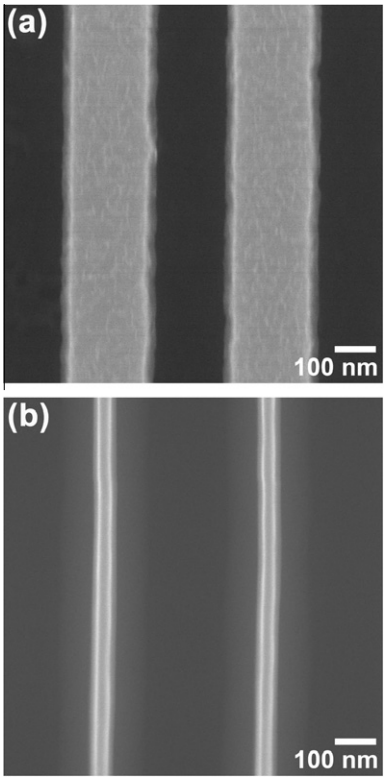

Fig. 3. SEM images of Si master features resized through thermal oxidation. (a) Unoxidized 226 nm Si lines fabricated by EBL. These lines were oxidized to a width of 356 nm (not shown) and then, (b) etched in BOE to remove the SiO_2 layer producing the 55 nm wide Si lines shown.

thickness of 59 nm. In an unpatterned region of the master, this SiO_2 thickness was explicitly measured by ellipsometry, and a value of 55 nm was recorded. This matches well with the oxide thickness estimated by SEM and the calculated SiO_2 thickness.

The oxidized 10 nm gap is ~40 times smaller than the length of the feature, which is generally considered difficult to achieve with direct EBL. While EBL has been used to achieve these geometries, a delicate balance of several interrelated process parameters (such as electron dose, write speed, resist thickness and uniformity, developer concentration and time, etc.) must be maintained, and the requirements generally become more stringent with increasing resolution. Tighter process control and increased EBL write times tend to be required as resolution targets are reduced. In addition, the oxidized 10 nm gap demonstrated here has a large height to gap width ratio (~30:1), and this ratio is difficult to obtain through direct RIE etching of an initial 10 nm gap.

Thermal oxidation can also be used to reduce the size of positive features as demonstrated in Fig. 3. With 46% of the SiO_2 layer formed beneath the original Si surface, thermal oxidation followed by SiO_2 etching results in the reduction of positive feature dimensions. In Fig. 3, a 226 ± 2 nm Si line was thermally oxidized to 356 ± 4 nm then etched in BOE, resulting in a 55 ± 1 nm Si line. One key benefit of this method is that since the surface free energy is proportional to the local radius of curvature (i.e., the Gibbs–Thomson relation), greater oxidation and etching rates are observed for rough surface features, and sidewall roughness tends to decrease during the oxidation/etching process [29–31].

Because the feature dimensions are directly related to oxide thickness, run-to-run reproducibility and cross-wafer uniformity are dominated by variability in the thermal oxidation process. Rapid thermal oxidation is known to be capable of generating high quality oxides with better than 3% uniformity across 200 mm wafers [38]. With our particular equipment, less uniformity was observed (15% across a 100 mm wafer, or 2% within a 25 mm radius of the center; see Supplementary data for thickness maps), and therefore, variation in feature sizes across a wafer is expected. Despite this, good run-to-run reproducibility (within ~3%) was attained via consistent placement of substrates within the annealing chamber, and any improvements to the oxide uniformity will directly lead to more consistent feature sizes. Another potential issue affecting pattern transfer fidelity is corner rounding of the features during the oxidation process. Rounded edge profiles can be observed in Fig. 4b–d, and these profiles are transferred to the NIL resist at the resist/wafer interface during the NIL process. To minimize the resulting aberrations, the radii at the corners of an oxidized master would ideally be a small fraction of the imprinted resist thickness. To best accomplish this, the required oxidative resizing should be minimized by using the highest initial EBL resolution reasonably achievable, or alternately, an anisotropic RIE could be performed post-oxidation to decrease the corner radii at all SiO_2 edges.

To demonstrate NIL pattern transfer with an oxidized master, we employed an interdigitated array as the NIL master. As shown in Fig. 4a, the array originally consisted of 500 nm lines separated by 166 ± 5 nm gaps. With successive thermal oxidations, the initial 166 nm gap width was thinned to 99 ± 4 nm with a 35 min oxidation (shown in Fig. 4b), 76 ± 3 nm with a 135 min oxidation (shown in Fig. 4c) and 39 ± 2 nm with a 205 min oxidation (shown in Fig. 4d). In the process, the gap width was reduced, while the pitch of the interdigitated array remained constant. Note that the relative standard deviation of the gap dimensions increased only slightly during oxidation (3–5%), indicating that feature shape was largely retained upon oxidation. Since the oxidized surface is OH-rich, attachment of a silane-based release agent was straightforward. The oxidized features were then transferred into the NIL

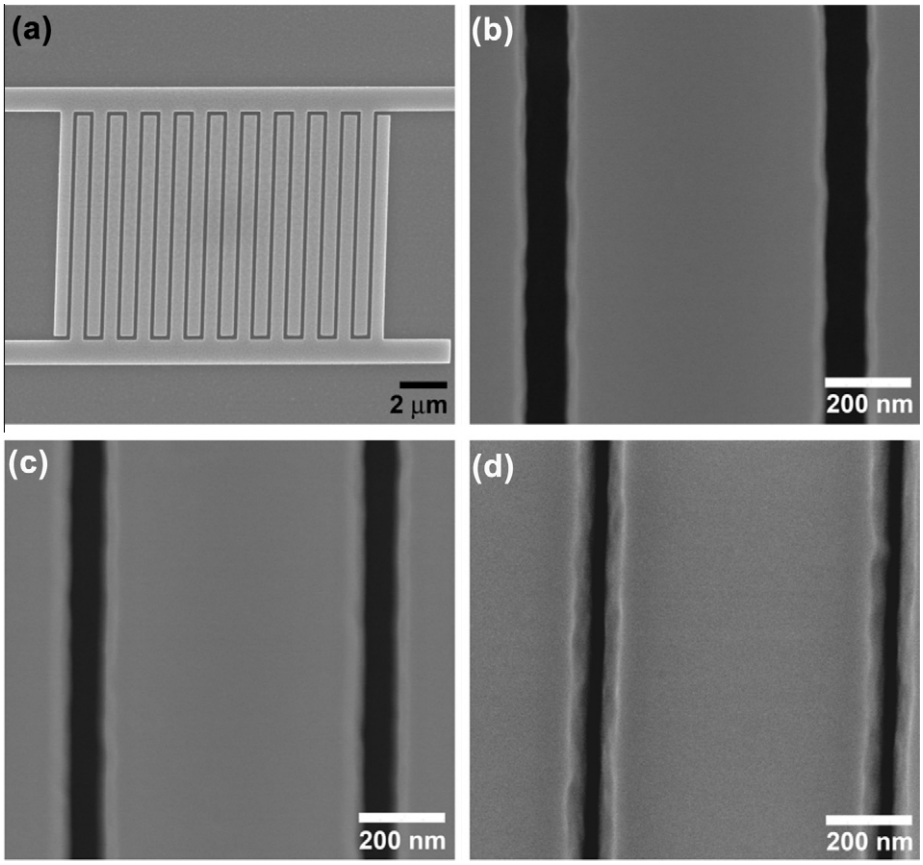

Fig. 4. Oxidation of an interdigitated array NIL master. (a) Original unoxidized interdigitated array master with 500 nm line widths and 166 nm gaps. The gaps are reduced to 99 nm (b), 76 nm (c), and 39 nm (d) through successive thermal oxidation processes.

resist by thermal NIL: the 166 and 39 nm features in Fig. 5a and b were transferred from the original and oxidized NIL masters in Fig. 4a and d, respectively. Qualitatively, the roughness of the transferred patterns is equivalent to that of the corresponding master.

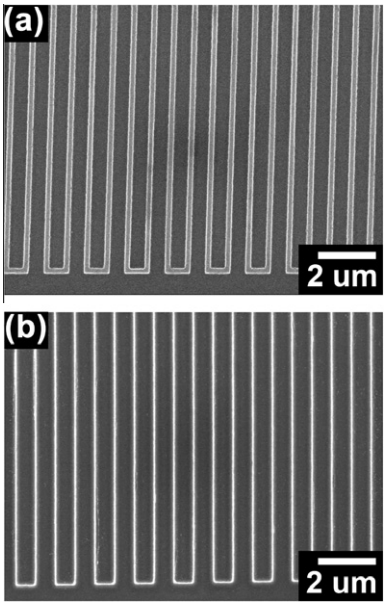

Fig. 5. SEM images demonstrating pattern transfer by NIL. (a) 166 nm features transferred from the Si master in Fig. 4a. (b) 39 nm features transferred from the oxidized master in Fig. 4d.

4. Conclusions

We have introduced a simple thermal oxidation approach to reduce the feature sizes of both positive and negative features on an NIL master. We explicitly demonstrate that negative structures can be thinned from 74 to 10 nm, while positive features can be reduced from 226 to 55 nm, but we expect the procedure to be capable of producing further resolution enhancements. Methods to improve this technique include *in situ* monitoring of SiO_2 growth, developing post-oxidation techniques to obtain sharper edge profiles, and advanced modeling of O_2 diffusion and SiO_2 growth rate in sub-10 nm trenches. The greatest advantage inherent to the technique is from a fabrication perspective: the ability to choose modest EBL patterns which are simple, fast and reliable to produce, followed by a post-process oxidation to reduce the feature sizes and create higher resolution masters.

Acknowledgements

Support for this work was provided by the National Science Foundation, Alberta Innovates: Technology Futures and the National Institute for Nanotechnology – National Research Council Canada. Tim Patrie is acknowledged for NIL and RTA support, Bryan Szeto and Scott Munro for advice on master fabrication and Daniel Salamon for SEM support.

Appendix A. Supplementary data

Supplementary data associated with this article can be found, in the online version, at doi:10.1016/j.mee.2011.08.006.

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